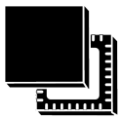
SPC2168 Datasheet

Dual Cortex-M4 core based MCU with 16 channel PWMs, 20 channel 14-bit ADC, 6 PGAs with Comparators

Features

- Dual ARM 32-bit Cortex-M4 CPU Core with FPU
  - Main Core and CAU (control accelerator unit)
  - Mailbox for dual core communication
  - 200 MHz maximum frequency
- Memories
  - Up to 512 KB embedded flash
  - 512 Bytes OTP flash
  - Up to 80 KB on-chip SRAM (including 16 KB XIP-Cache)
- Clock, reset and supply management
  - Single 3.3 V power supply
  - POR, Brown-out detector (BOD)
  - 1-to-66 MHz external crystal oscillator
  - Two internal 32MHz factory-trimmed RC
  - PLL for CPU clock
- 6-channel DMA controller
- 14-bit A/D converters (up to 20 channels)
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Programmable gain amplifier (PGA)
  - 6 integrated internal PGAs
  - Programmable Gains
    Single-ended: 1, 2, 4, 8, 12, 16, 24, 32
    Differential: 2, 4, 8, 16, 24, 32, 48, 64
- Analog comparator
  - 16 high-speed comparators
  - Output with digital deglitch filter

LQFP80 (12 x 12 mm)
LQFP64 (10 x 10 mm)
LQFP52 (14 x 14 mm)
LQFP48 (7 x 7 mm)



QFN52 (6 x 6 mm)

  - 6 DACs as reference
  - Out of range voltage protection
  - Phase comparison
- PWM
  - 8 enhanced PWM modules
  - 16 PWM outputs in total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 61 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 7 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - Two SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1，SPI x 1，I2C x 1
- Security Modules
  - CRC x 1, AES x 1, 64-bit unique ID

- Operating temperature
  - ➢ Junction temperature: -40 to +125 °C
  - ➢ Ambient temperature: -40 to +105 °C

Table 1-1: SPC2168 device features and peripheral counts

Peripheral	SPC2168(L/Z)APE80	SPC2168(L)APE64	SPC2168APE52	SPC2168APE48	SPC2168API52
Flash	512KB 256KB (L) 128KB (Z)	512KB 256KB (L)	512KB	512KB	512KB
OTP Flash	512Bytes	512Bytes	512Bytes	512Bytes	512Bytes
SRAM	80KB	80KB	80KB	80KB	80KB
DMA Number of channels	1 6 channels	1 6 channels	1 6 channels	1 6 channels	1 6 channels
GPIOs[1]	61	49	42	38	40
14-bit ADC Number of channels	1 20 channels	1 17 channels	1 16 channels	1 14 channels	1 18 channels
PGA	6	6	6	6	6
Analog comparators	16	16	16	16	16
DAC	6	6	6	6	6
PWM Number of channels	8 16 channels	8 16 channels	8 12 channels	8 12 channels	8 10 channels
ECAP	1	1	1	1	1
General-purpose timers	3	3	3	3	3
Watchdog timers	2	2	2	2	2
AES	1	1	1	1	1
CRC	1	1	1	1	1
UART	1	1	1	1	1
SPI	1	1	1	1	1
I2C	1	1	1	1	1
Maximum f_{CPU}	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz

[1] Not including GPIO47 (BOOT) pin.

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Revision history

Version	Date	Author	Status	Changes
1	2019-04-01	–	Outdated	1. Initial version.
2	2019-08-16	–	Outdated	1. Modifies JTAG pin description in Table 3-1.
3	2019-12-20	–	Outdated	1. Add Table 5-18. 2. Add Table 5-19.
4	2020-05-12	–	Outdated	1. Update Section 2.9 for boot mode description. 2. Update Section 2.16 and modify the maximum speed of SPI. 3. Update Table 5-3. 4. Update Table 5-7. 5. Update Figure 5-2. 6. Add Table 5-8. 7. Add Table 5-9. 8. Add Table 5-10. 9. Add Table 5-11. 10. Update Table 5-12. 11. Add Table 5-21. 12. Add Table 5-26.
5	2020-05-22	–	Outdated	1. Update Section 2.20 for phase comparison. 2. Add Figure 3-2. 3. Add Table 3-2. 4. Add Figure 3-5. 5. Add Table 3-5. 6. Add Figure 6-3. 7. Add Table 6-2. 8. Add Figure 6-4. 9. Add Figure 6-9. 10. Add Table 6-5. 11. Add Table 7-1.
6	2020-07-06	–	Outdated	1. Update Section 2.9 for boot mode description. 2. Update Section 2.14 for UART features. 3. Update Section 2.23 for CRC features. 4. Update Table 5-13 and modify the value of R_{IN} parameter.
7	2020-07-31	–	Outdated	1. Add Figure 5-3. 2. Update Table 5-13. 3. Update Table 5-17.
8	2020-10-08	–	Outdated	1. Update Table 5-3. 2. Add characteristics of ambient temperature T_A.

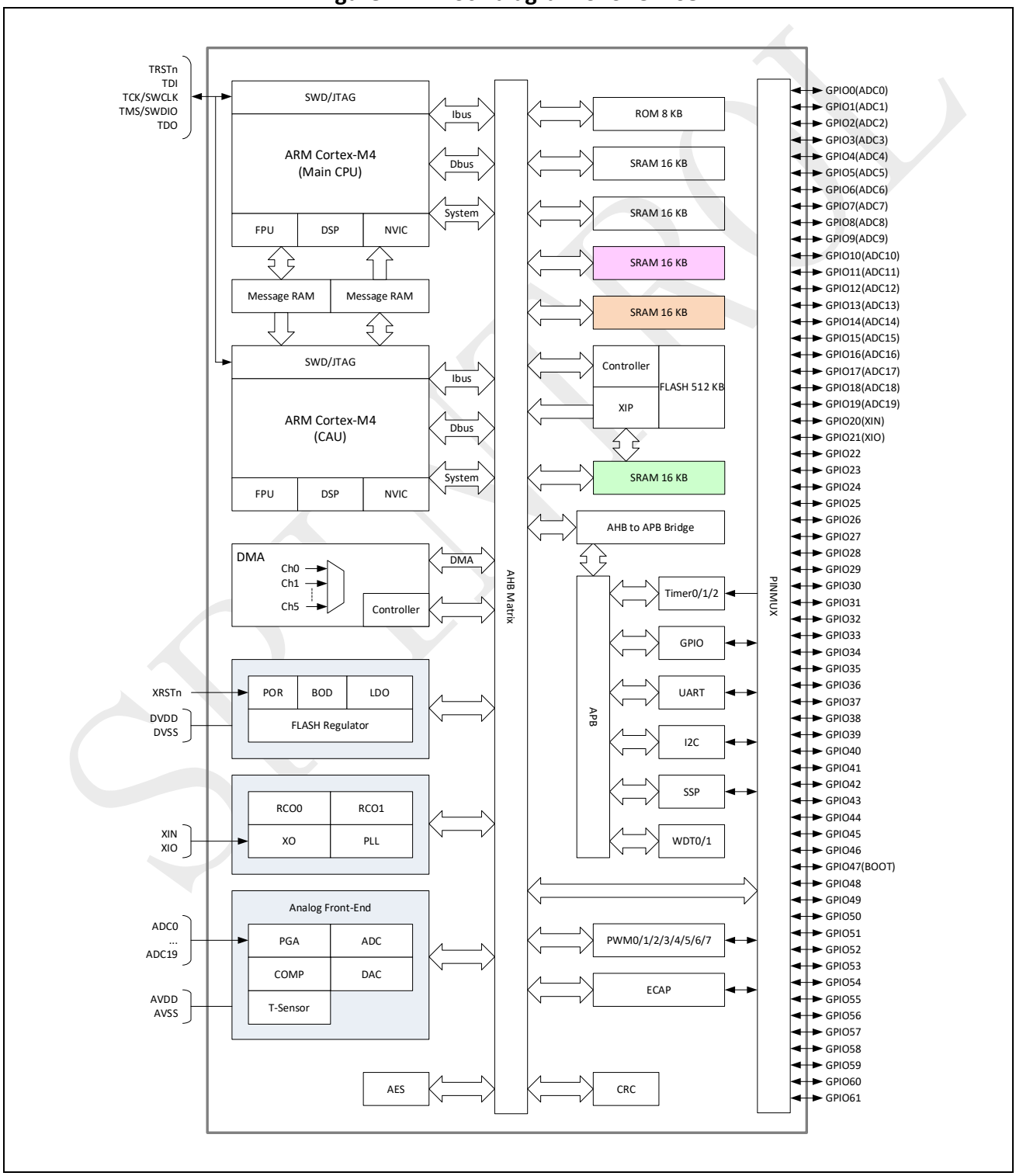
Version	Date	Author	Status	Changes
				3. Update Section 2.14 for UART features. 4. Update Table 5-13.
9	2021-03-28	–	Outdated	1. Add current data for low and high temperature in Table 5-4, Table 5-5 and Table 5-6. 2. Add Figure 6-10. 3. Add SPC2168 LQFP52 pin description and package information. 4. Add SPC2168 LQFP48 pin description and package information. 5. Update Figure 3-2. 6. Update comparator pin descriptions in Table 3-1 ~ Table 3-5. 7. Add Table 3-6 and Table 3-7. 8. Add Table 3-8. 9. Add note for Table 5-4. 10. Add note for Table 5-5. 11. Update Table 5-6. 12. Update chip communication interface features. 13. Update Figure 3-1 and its notes. 14. Update Figure 3-2 and its notes. 15. Update Figure 3-3 and its notes. 16. Update Figure 3-4 and its notes. 17. Update Figure 3-5 and its notes.
10	2021-11-27	–	Outdated	1. Add Table 1-1. 2. Add Table 5-20. 3. Update Table 3-6. 4. Update Section 2.11. 5. Update Table 5-14. 6. Add Figure 5-4. 7. Add Figure 5-5. 8. Add Figure 5-6. 9. Add Figure 5-7. 10. Update Table 3-1, modify the description for debug pins. 11. Update Table 3-2, modify the description for debug pins. 12. Update Table 3-3, modify the description for debug pins. 13. Update Table 3-4, modify the description for debug pins. 14. Update Table 3-5, modify the description for debug pins.

Version	Date	Author	Status	Changes
				15. Update deep-sleep current consumption value in Table 5-4.
11	2022-11-21	–	Outdated	1. Update Section 2.23. 2. Update Table 5-3, remove parameter I_{OZ}. 3. Update Table 1-1 and Table 7-1. 4. Update Section 2.9 and Section 2.10. 5. Update Conditions of parameter R_{PU} and R_{PD} in Table 5-3. 6. Update Table 3-6. 7. Update Table 3-7. 8. Update Section 2.6.
C/0	2024-08-09	J. Zhou	Outdated	1. Update the document style. 2. Update Section 2.14. 3. Update Figure 3-4 pin layout. 4. Update the pin definition in Table 3-4.
C/1	2024-10-30	J. Zhou	Outdated	1. Update Figure 4-1、Figure 4-2. 2. Add thermal resistance characteristics for different packages. 3. Add performance description for DAC waveform generation.
C/2	2025-05-20	J. Zhou	Outdated	1. Update f_{RCO} in Table 5-9. 2. Update Figure 4-1 and Figure 4-2.
C/3	2025-09-23	J. Zhou	Outdated	1. Add Figure 1-2 to illustrate the resource access permissions for the dual cores. 2. Add a description of the SRAM address allocation in Section 4. 3. Correct the high-speed mode data rate in Section 2.15. 4. Update Table 5-9.
C/4	2026-07-10	J. Zhou	Outdated	1. Update the functional description of the pre-programmed IO module. 2. Add Important Statement and Disclaimer. 3. Add Figure 2-1 in Section 2.8. 4. Add Section 7.1.
C/5	2026-08-04	J. Zhou	Released	1. Delete pre-programmed IO module (SIO).

1 Device overview

The SPC2168 device from Spintrol is a dual core, high performance and integration system-on-chip (SOC) microcontroller. The SPC2168 incorporates two 32-bit ARM Cortex-M4 high-performance processors with a software-programmable clock rate as high as 200 MHz, 80 KB SRAM, embedded flash with 512 KB, and an extensive range of enhanced I/Os and peripherals. Figure 1-1 shows the functional block diagram for the SPC2168.

Figure 1-1: Block diagram of SPC2168



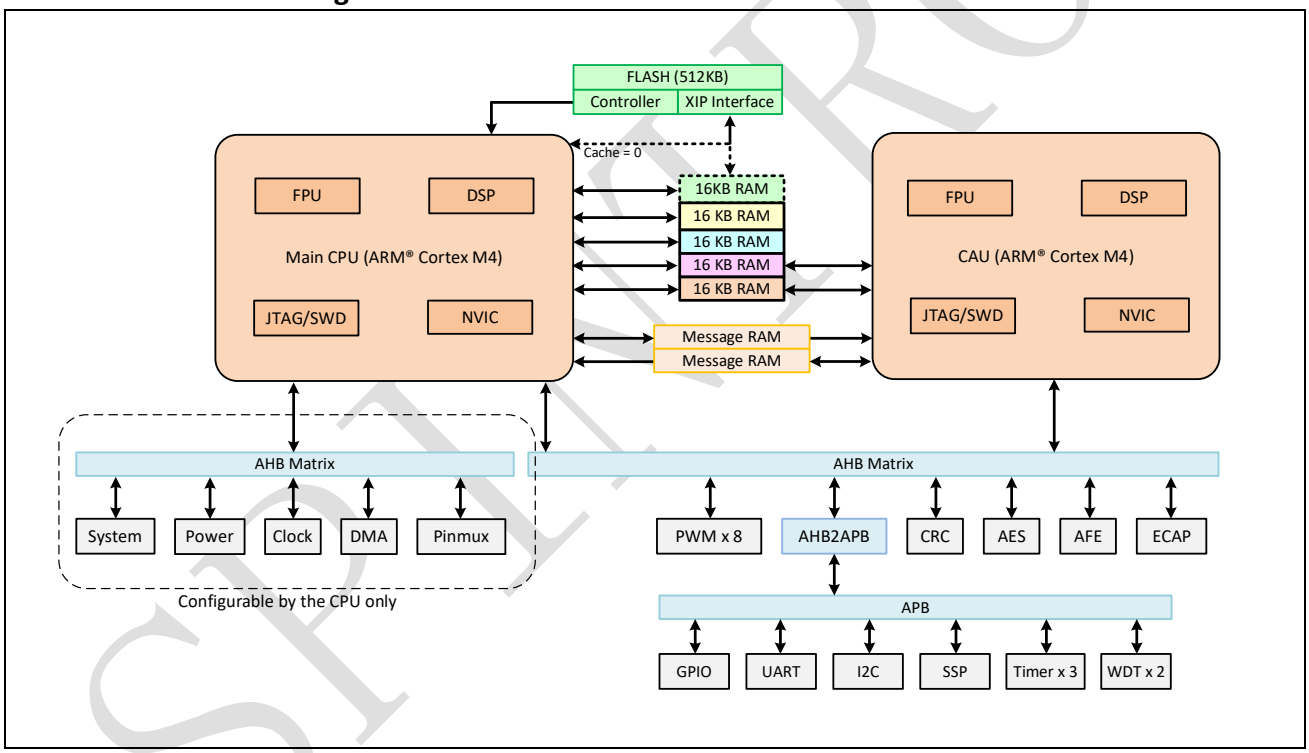
The SPC2168 Mailbox completes messages communication between Main CPU and Control Accelerator Unit (CAU). Main CPU sends messages through interrupt to CAU and when CAU receives messages successfully, it also sends confirmation messages to Main CPU by interruption, and vice versa.

The Direct Memory Access Controller (DMAC) is used to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMAC without any CPU actions. This keeps CPU resources free for other operations.

The SPC2168 device offers a 14-bit ADC, 6 PGAs, 8 enhanced PWMs, 3 general purpose 32-bit timers, as well as standard and advanced communication interface: UART, I^2C and SPI. These features make the SPC2168 ideal for motion control application.

The SPC2168 operates from a 2.97 to 3.63 V power supply. The temperature range is from -40 °C to +125 °C temperature range. The package type can be 80-pin LQFP, 64-pin LQFP, 48-pin LQFP or 52-pin QFN/LQFP.

Figure 1-2: Main CPU and CAU Accessible Resources



As shown in Figure 1-2, there are certain areas that can only be accessed by the Main CPU and are inaccessible to the CAU. These include the Flash, portions of the RAM, as well as write operations to the System, Power, Clock, DMA, and Pinmux registers. For details regarding dual-core access to the RAM, refer to Section 4.

2 Feature descriptions

2.1 Dual ARM Cortex-M4 core with FPU

The SPC2168 integrates two full-feature ARM Cortex-M4 core with FPU that can runs up to 200 MHz, is therefore compatible with all ARM tools and software. The Main CPU completes the power supply, reset and BOOT management of the whole chip. According to the load characteristics of the processor thread, the CAU can also take on the specific motor control task, thus improving the real-time and security performance of the system in a close step.

2.2 Embedded SRAM

The SPC2168 has implemented 80KB (include XIP Cache) SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states. A 16KB storage unit can be used as XIP Cache or SRAM.

2.3 Embedded Flash memory

Up to 512 KB of embedded Flash memory is available for storing code and data.

2.4 Nested vectored interrupt controller (NVIC)

Each CPU in SPC2168 embeds a nested vectored interrupt controller able to handle up to 63 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPC2168 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply and Reset

The SPC2168 supports nominal 3.3V single power supply, which powers the IOs, internal voltage regulators and analog circuitry on chip.Supply ramp-up rate less than or equal 0.015 V/us.

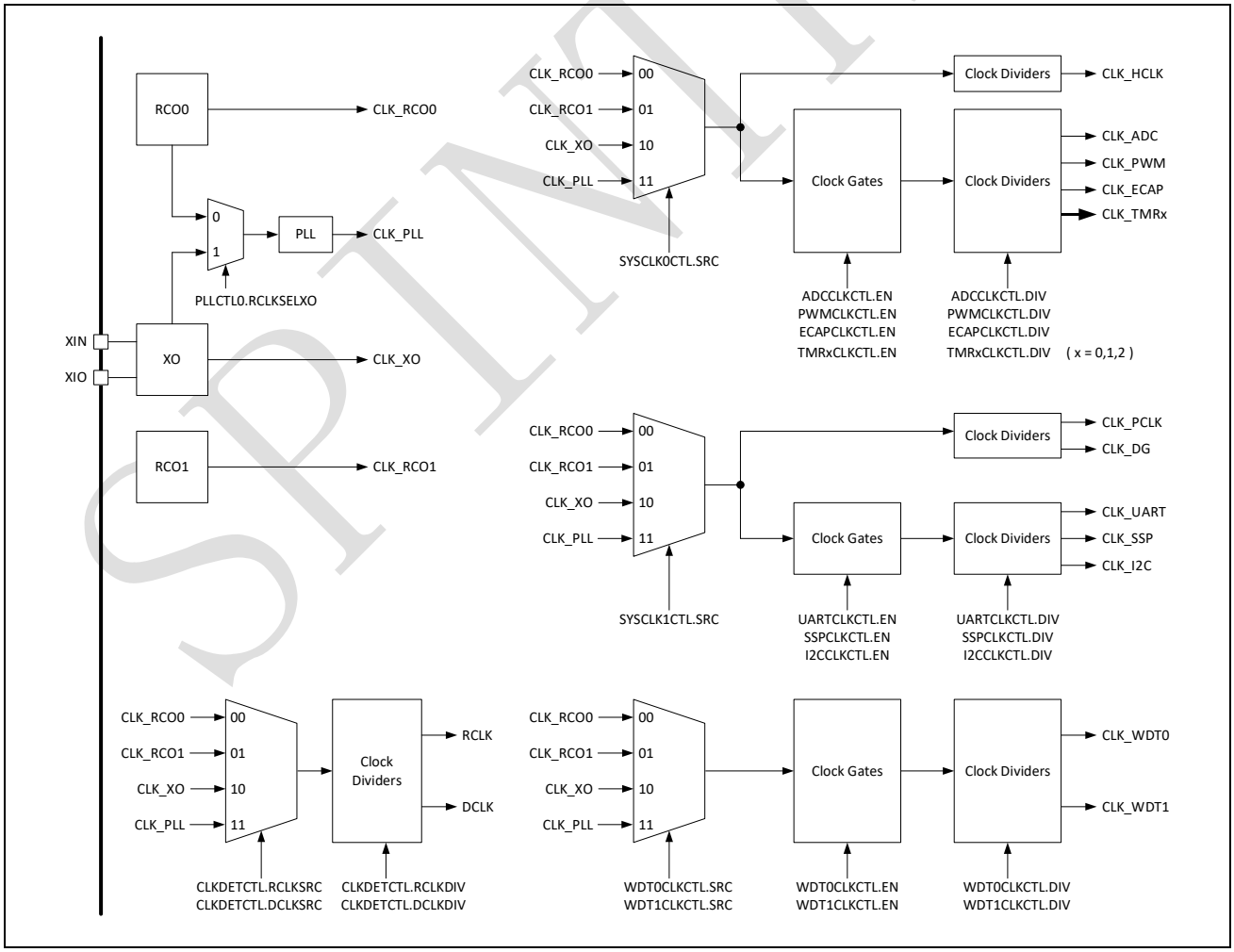
The SPC2168 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the 3.3V/1.2V domain power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when voltage of the power domain is higher or drops below the pre-set value. The interrupt service routine then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.8 Clocks

Figure 2-1: Clock tree



System clock selection is performed on startup. The internal 32 MHz RC oscillator is selected by default upon reset. An external 1 - 66 MHz oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The output frequency covers from 25 MHz to 200 MHz.

Several clock dividers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency is 200 MHz for AHB and 50 MHz for APB. See Figure 2-1 for details on the clock tree.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor begins code execution from this ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (boot pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, for chip with LQFP48 or QFN52 package, the GPIO38 is configured as UART_TXD and the GPIO39 is configured as UART_RXD; for chip with other packages, the GPIO44 is configured as UART_TXD and the GPIO45 is configured as UART_RXD.

Note:
1. The boot pin should always keep high when chip normally running.
2. The TRSTn pin is recommended to set as low.
3. When TRSTn is high, the related debug interface pins (GPIO48 ~ GPIO51) must not be used as GPIO function.

2.10 General-purpose IOs (GPIOs)

The SPC2168 can be configured to support as many as 61 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

2.11 Direct memory access controller (DMAC)

The DMA controller in SPC2168 has 6 channels in total to manage memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests. The DMA controller is interconnected with DRAM through the AHB bus matrix as well as APB peripherals (UART and SSP) through AHB-to-APB bridge. It features:

- 6 independently configurable channels and each channel FIFO depth is 16 x 32 bits
- Programmable transfer type for each channel: memory-to-memory, memory-to-peripheral and peripheral-to-memory
- Programmable source and destination addresses: address increment, decrement, or no change.

- Single block transfer with configurable block size up to 4095 words (32 bits)
- 4 configurable hardware handshaking interfaces

2.12 Mailbox

Mailbox completes messages communication between Main CPU and CAU. The Mailbox includes two message RAMs and two interrupt trigger units. The message RAMs are always mapped to both Main CPU and CAU memory spaces and can be accessed by byte, half-word and word. The size of each message RAM is 64 x 32 bits.

- CAU to Main CPU Message RAM

  The CAU can use this block memory to pass data to the Main CPU. The block is both readable and writable by the CAU. This block is also readable by the Main CPU but writes by the Main CPU are ignored.

- Main CPU to CAU Message RAM

  The Main CPU can use this block memory to pass data to the CAU. This message RAM is both readable and writable by the Main CPU. This block is also readable by the CAU but writes by the CAU are ignored.

  The interrupt trigger units are used for event indication between the Main CPU and the CAU.

2.13 Timers and watchdogs

The SPC2168 device includes three general-purpose timers, two watchdog timers and two SysTick timers (one for each CPU).

General-purpose timers

The SPC2168 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPC2168 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter

- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.14 UART

The SPC2168 has an UART module. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5~8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 12.5 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.15 I^2C

The I^2C bus interface complies with the common I^2C protocol. It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.16 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 50 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase

- Transmit and receive FIFOs

2.17 ADC

One 14-bit analog-to-digital converter is embedded into SPC2168 and has up to 20 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has three independent built-in sample-and-hold (S/H). Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 14-bit resolution
- 140 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Triple-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input short and disconnection detection for safety

Please see Table 5-12 for ADC characteristics.

2.18 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.19 PGAs

Six flexible programmable gain amplifiers (PGAs) are embedded into SPC2168 and shares up to 20 channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains

  Differential mode: 2, 4, 8, 16, 24, 32, 48, 64; Single-ended mode: 1, 2, 4, 8, 12, 16, 24, 32.

- Settling time: 400 ns to 800 ns

Please see Table 5-13 for PGA characteristics.

2.20 Analog comparators

The SPC2168 has sixteen high-speed comparators. Each comparator use the internal DAC as reference to monitor whether the PGA inputs or outputs exceed the threshold. A DAC can be used to generate a static voltage as a threshold for the somparator, but does not guarantee the performance of the waveform. Two comparators are designed for each PGA. One is monitoring too-high voltage, the other is monitoring too-low voltage. The extra two pairs of comparators are reserved for additional applications. The comparator output is routed to the PWM Trip-Zone modules. Additionally, each comparator can implement the phase comparison for motor commutation. The detail channel selection can be referred to Technical Reference Manual.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter
- Phase comparison

Please see Table 5-14 and Table 5-15 for analog comparator and DAC characteristics.

2.21 PWMs

The SPC2168 integrates 8 PWM modules and supports 16 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.22 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPC2168 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.23 Cyclic redundancy check (CRC)

The SPC2168 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Five CRC standard polynomials supported

2.24 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128-, 192-, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

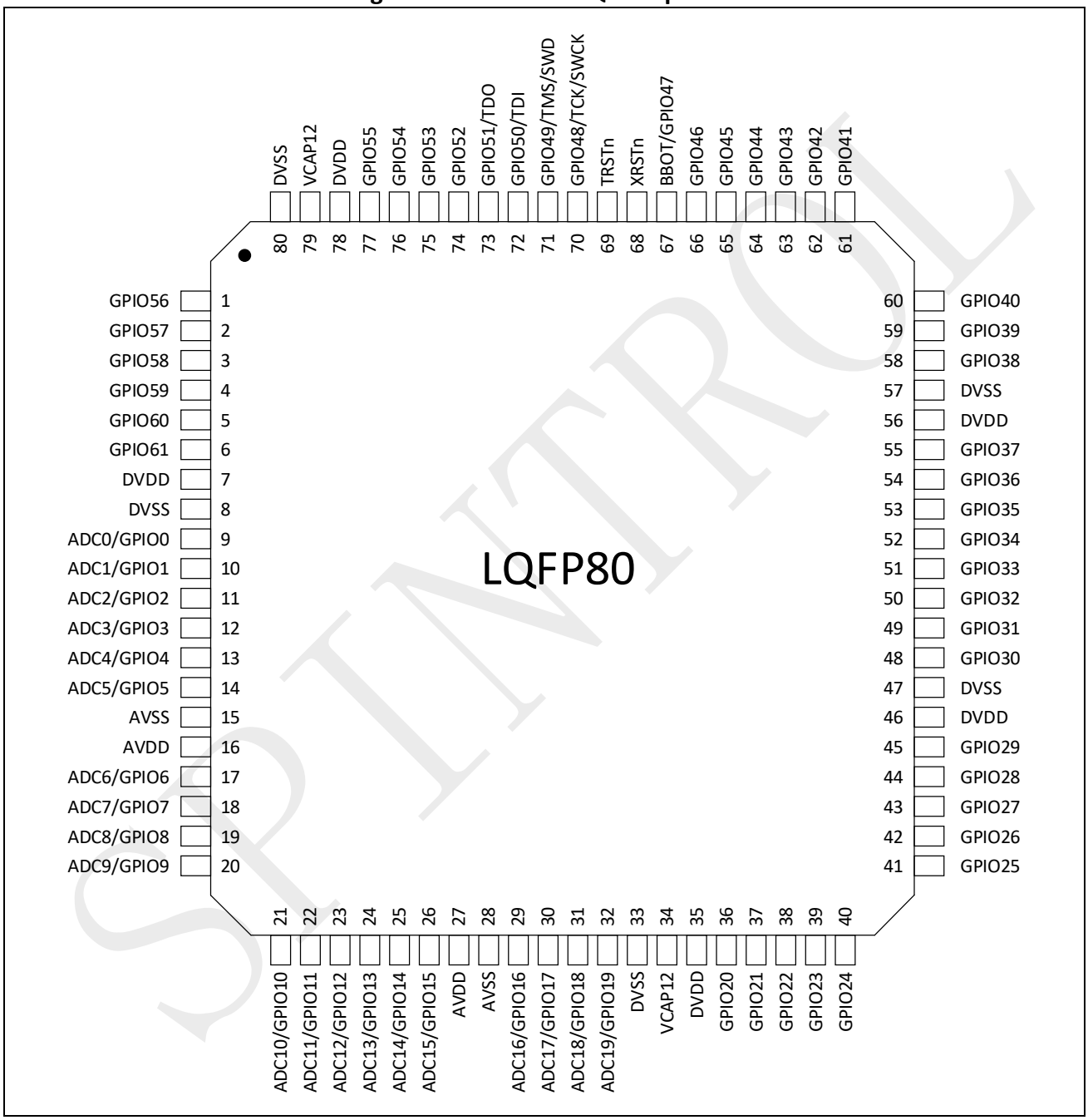
2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPC2168 certain security feature. Dual SWD interfaces can be enabled for ease of the main CPU and CAU co-debug.

3 Pinouts and pin description

3.1 LQFP80

Figure 3-1: SPC2168 LQFP80 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO48 ~ GPIO51 pins work as Debug interface and can't be configured as other functions.

Table 3-1: SPC2168 LQFP80 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO56	I/O	General-purpose input/output 56
	PWM4A	O	PWM4 output A
2	GPIO57	I/O	General-purpose input/output 57
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B
3	GPIO58	I/O	General-purpose input/output 58
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
4	GPIO59	I/O	General-purpose input/output 59
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
5	GPIO60	I/O	General-purpose input/output 60
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
6	GPIO61	I/O	General-purpose input/output 61
	PWM6B	O	PWM6 output B
7	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
8	DVSS	S	Digital ground
9	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
10	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
11	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
12	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
13	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
14	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
15	AVSS	S	Analog ground
16	AVDD	S	Analog power, add 4.7uF and 0.1uF bypass ceramic cap to AVSS
17	GPIO6	I/O	General-purpose input/output 6
	ADC6	AI	ADC channel 6 input
18	GPIO7	I/O	General-purpose input/output 7

Pin	Signal	Type[1]	Description
	ADC7	AI	ADC channel 7 input
19	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
20	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
21	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	COMP3H	O	Comparator COMP3H result output
22	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	COMP3L	O	Comparator COMP3L result output
	DCLK	O	Clock output from CLKDET module for monitoring
23	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	COMP4H	O	Comparator COMP4H result output
24	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	COMP4L	O	Comparator COMP4L result output
25	GPIO14	I/O	General-purpose input/output 14
	ADC14	AI	ADC channel 14 input
	COMP5H	O	Comparator COMP5H result output
26	GPIO15	I/O	General-purpose input/output 15
	ADC15	AI	ADC channel 15 input
	COMP5L	O	Comparator COMP5L result output
27	AVDD	S	Analog power, add 4.7uF and 0.1uF bypass ceramic cap to AVSS
28	AVSS	S	Analog ground
29	GPIO16	I/O	General-purpose input/output 16
	ADC16	AI	ADC channel 16 input
	COMP6H	O	Comparator COMP6H result output
30	GPIO17	I/O	General-purpose input/output 17
	ADC17	AI	ADC channel 17 input
	COMP6L	O	Comparator COMP6L result output
31	GPIO18	I/O	General-purpose input/output 18
	ADC18	AI	ADC channel 18 input
	COMP7H	O	Comparator COMP7H result output
32	GPIO19	I/O	General-purpose input/output 19
	ADC19	AI	ADC channel 19 input
	COMP7L	O	Comparator COMP7L result output
33	DVSS	S	Digital ground
34	VCAP12	S	1.2V power, add 2.2uF bypass ceramic cap to DVSS
35	DVDD	S	Digital power, add 4.7uF and 0.1uF ceramic cap to DVSS
36	GPIO20	I/O	General-purpose input/output 20

Pin	Signal	Type[1]	Description
	XIN	AI	External oscillator input
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I²C clock
	UART_TXD	O	UART transmit data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
37	GPIO21	I/O	General-purpose input/output 21
	XIO	AI/O	External oscillator input or output
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I²C data
	UART_RXD	I	UART receive data
	PWMSOC[2]	O	PWM SOC signal output for monitoring
38	GPIO22	I/O	General-purpose input/output 22
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
39	GPIO23	I/O	General-purpose input/output 23
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
40	GPIO24	I/O	General-purpose input/output 24
	COMP0H	O	Comparator COMP0H result output
	PWM1A	O	PWM1 output A
41	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM2A	O	PWM2 output A
	PWM1B	O	PWM1 output B
42	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM3A	O	PWM3 output A
	PWM2A	O	PWM2 output A
43	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM1B	O	PWM1 output B
	PWM2B	O	PWM2 output B
44	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM2B	O	PWM2 output B
	PWM3A	O	PWM3 output A
45	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM3B	O	PWM3 output B
46	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
47	DVSS	S	Digital ground
48	GPIO30	I/O	General-purpose input/output 30
	I2C_SCL	I/O	I²C clock

Pin	Signal	Type[1]	Description
49	GPIO31	I/O	General-purpose input/output 31
	I2C_SDA	I/O	I^2C data
50	GPIO32	I/O	General-purpose input/output 32
	COMP3H	O	Comparator COMP3H result output
	PWM4A	O	PWM4 output A
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
51	GPIO33	I/O	General-purpose input/output 33
	COMP3L	O	Comparator COMP3L result output
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B
	PWMSOC[2]	O	PWM SOC signal output for monitoring
52	GPIO34	I/O	General-purpose input/output 34
	COMP4H	O	Comparator COMP4H result output
	PWM0A	O	PWM0 output A
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
53	GPIO35	I/O	General-purpose input/output 35
	COMP4L	O	Comparator COMP4L result output
	PWM0B	O	PWM0 output B
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
54	GPIO36	I/O	General-purpose input/output 36
	COMP5H	O	Comparator COMP5H result output
	PWM7A	O	PWM7 output A
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
55	GPIO37	I/O	General-purpose input/output 37
	COMP5L	O	Comparator COMP5L result output
	PWM7B	O	PWM7 output B
	PWM6B	O	PWM6 output B
56	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
57	DVSS	S	Digital ground
58	GPIO38	I/O	General-purpose input/output 38
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWMSOCA	O	PWM SOCA signal output for monitoring
59	GPIO39	I/O	General-purpose input/output 39
	SPI_SFRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWMSOCB	O	PWM SOCB signal output for monitoring
60	GPIO40	I/O	General-purpose input/output 40

Pin	Signal	Type[1]	Description
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I^2C clock
	PWMSOCC	O	PWM SOCC signal output for monitoring
61	GPIO41	I/O	General-purpose input/output 41
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I^2C data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
62	GPIO42	I/O	General-purpose input/output 42
	I2C_SCL	I/O	I^2C clock
	COMP6H	O	Comparator COMP6H result output
	SPI_SCLK	I/O	SPI clock input/output
63	GPIO43	I/O	General-purpose input/output 43
	I2C_SDA	I/O	I^2C data
	COMP6L	O	Comparator COMP6L result output
	SPI_SFRM	I/O	SPI frame signal
64	GPIO44	I/O	General-purpose input/output 44
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	COMP7H	O	Comparator COMP7H result output
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
65	GPIO45	I/O	General-purpose input/output 45
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	COMP7L	O	Comparator COMP7L result output
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
66	GPIO46	I/O	General-purpose input/output 46
67	BOOT (GPIO47)	I/O	Boot pin (General-purpose input/output 47)
68	XRSTn	I	Device reset pin, reset the device when low
69	TRSTn	I	JTAG reset pin, reset the JTAG when low
70	GPIO48	I/O	General-purpose input/output 48
	TCK/SWCK	I	JTAG clock or SWD clock
	COMP0H	O	Comparator COMP0H result output
	COMP3H	O	Comparator COMP3H result output
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
71	GPIO49	I/O	General-purpose input/output 49
	TMS/SWD	I/O	JTAG mode select or SWD data
	COMP0L	O	Comparator COMP0L result output
	COMP3L	O	Comparator COMP3L result output

Pin	Signal	Type[1]	Description
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
72	GPIO50	I/O	General-purpose input/output 50
	TDI	I	JTAG data input
	SWCK(CAU)	I	SWD clock for CAU
	COMP1H	O	Comparator COMP1H result output
	COMP4H	O	Comparator COMP4H result output
	Note: when TRSTn is HIGH, this pin always works as TDI or SWCK(CAU) and can't be configured as other functions.		
73	GPIO51	I/O	General-purpose input/output 51
	TDO	O	JTAG data output
	SWD(CAU)	I/O	SWD data for CAU
	COMP1L	O	Comparator COMP1L result output
	COMP4L	O	Comparator COMP4L result output
	Note: when TRSTn is HIGH, this pin always works as TDO or SWD(CAU) and can't be configured as other functions.		
74	GPIO52	I/O	General-purpose input/output 52
	PWM0A	O	PWM0 output A
	COMP2H	O	Comparator COMP2H result output
	COMP5H	O	Comparator COMP5H result output
75	GPIO53	I/O	General-purpose input/output 53
	PWM0B	O	PWM0 output B
	COMP2L	O	Comparator COMP2L result output
	COMP5L	O	Comparator COMP5L result output
76	GPIO54	I/O	General-purpose input/output 54
	PWM7A	O	PWM7 output A
	PWM4A	O	PWM4 output A
77	GPIO55	I/O	General-purpose input/output 55
	PWM7B	O	PWM7 output B
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B
78	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
79	VCAP12	S	1.2V power, add 0.1uF bypass ceramic cap to DVSS
80	DVSS	S	Digital ground

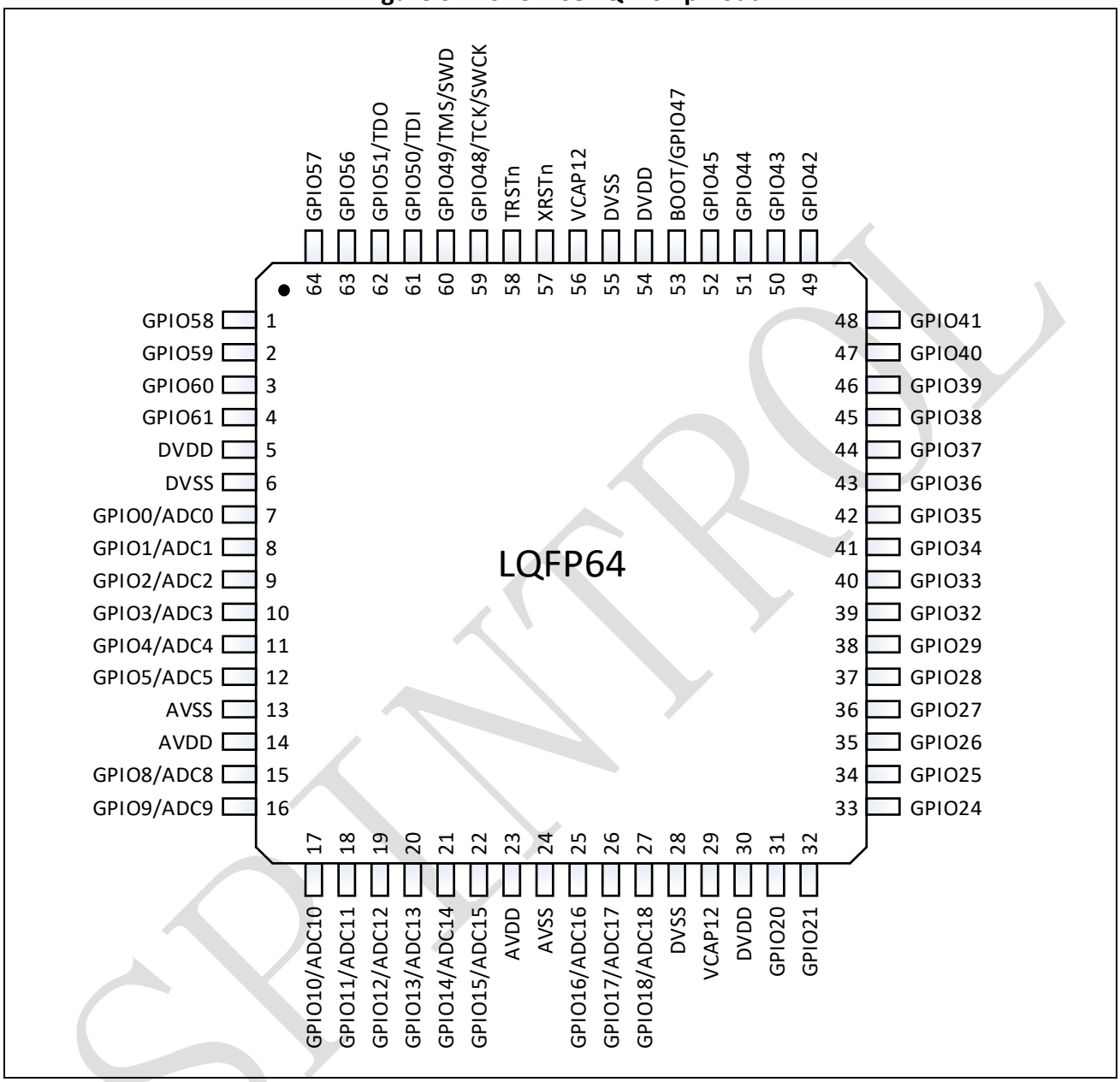
[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] PWMSOC signal is logic OR of PWMSOCA, PWMSOCB and PWMSOCC signal.

[3] All GPIO pins can be configured as ECAP input or output.

3.2 LQFP64

Figure 3-2: SPC2168 LQFP64 pinout



[1] The figure above shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO48 ~ GPIO51 pins work as Debug interface and can't be configured as other functions.

Table 3-2: SPC2168 LQFP64 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO58	I/O	General-purpose input/output 58
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
2	GPIO59	I/O	General-purpose input/output 59
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
3	GPIO60	I/O	General-purpose input/output 60
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
4	GPIO61	I/O	General-purpose input/output 61
	PWM6B	O	PWM6 output B
5	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
6	DVSS	S	Digital ground
7	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
8	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
9	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
10	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
11	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
12	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
13	AVSS	S	Analog ground
14	AVDD	S	Analog power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
15	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
16	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
17	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	COMP3H	O	Comparator COMP3H result output
18	GPIO11	I/O	General-purpose input/output 11

Pin	Signal	Type[1]	Description
	ADC11	AI	ADC channel 11 input
	COMP3L	O	Comparator COMP3L result output
	DCLK	O	Clock output from CLKDET module for monitoring
19	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	COMP4H	O	Comparator COMP4H result output
20	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	COMP4L	O	Comparator COMP4L result output
21	GPIO14	I/O	General-purpose input/output 14
	ADC14	AI	ADC channel 14 input
	COMP5H	O	Comparator COMP5H result output
22	GPIO15	I/O	General-purpose input/output 15
	ADC15	AI	ADC channel 15 input
	COMP5L	O	Comparator COMP5L result output
23	AVDD	S	Analog power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
24	AVSS	S	Analog ground
25	GPIO16	I/O	General-purpose input/output 16
	ADC16	AI	ADC channel 16 input
	COMP6H	O	Comparator COMP6H result output
26	GPIO17	I/O	General-purpose input/output 17
	ADC17	AI	ADC channel 17 input
	COMP6L	O	Comparator COMP6L result output
27	GPIO18	I/O	General-purpose input/output 18
	ADC18	AI	ADC channel 18 input
	COMP7H	O	Output of comparator 7 of high-voltage
28	DVSS	S	Digital ground
29	VCAP12	S	1.2V power, add 2.2uF bypass ceramic cap to DVSS
30	DVDD	S	Digital power, add 4.7uF and 0.1uF ceramic cap to DVSS
31	GPIO20	I/O	General-purpose input/output 20
	XIN	AI	External oscillator input
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	UART_TXD	O	UART transmit data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
32	GPIO21	I/O	General-purpose input/output 21
	XIO	AI/O	External oscillator input or output
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	UART_RXD	I	UART receive data
	PWMSOC[2]	O	PWM SOC signal output for monitoring
33	GPIO24	I/O	General-purpose input/output 24

Pin	Signal	Type[1]	Description
	COMP0H	O	Comparator COMP0H result output
	PWM1A	O	PWM1 output A
34	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM2A	O	PWM2 output A
	PWM1B	O	PWM1 output B
35	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM3A	O	PWM3 output A
	PWM2A	O	PWM2 output A
36	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM1B	O	PWM1 output B
	PWM2B	O	PWM2 output B
37	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM2B	O	PWM2 output B
	PWM3A	O	PWM3 output A
38	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM3B	O	PWM3 output B
39	GPIO32	I/O	General-purpose input/output 32
	COMP3H	O	Comparator COMP3H result output
	PWM4A	O	PWM4 output A
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
40	GPIO33	I/O	General-purpose input/output 33
	COMP3L	O	Comparator COMP3L result output
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B
	PWMSOC[2]	O	PWM SOC signal output for monitoring
41	GPIO34	I/O	General-purpose input/output 34
	COMP4H	O	Comparator COMP4H result output
	PWM0A	O	PWM0 output A
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
42	GPIO35	I/O	General-purpose input/output 35
	COMP4L	O	Comparator COMP4L result output
	PWM0B	O	PWM0 output B
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
43	GPIO36	I/O	General-purpose input/output 36
	COMP5H	O	Comparator COMP5H result output
	PWM7A	O	PWM7 output A

Pin	Signal	Type[1]	Description
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
44	GPIO37	I/O	General-purpose input/output 37
	COMP5L	O	Comparator COMP5L result output
	PWM7B	O	PWM7 output B
	PWM6B	O	PWM6 output B
45	GPIO38	I/O	General-purpose input/output 38
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWMSOCA	O	PWM SOCA signal output for monitoring
46	GPIO39	I/O	General-purpose input/output 39
	SPI_SFRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWMSOCB	O	PWM SOCB signal output for monitoring
47	GPIO40	I/O	General-purpose input/output 40
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I^2C clock
	PWMSOCC	O	PWM SOCC signal output for monitoring
48	GPIO41	I/O	General-purpose input/output 41
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I^2C data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
49	GPIO42	I/O	General-purpose input/output 42
	I2C_SCL	I/O	I^2C clock
	COMP6H	O	Comparator COMP6H result output
	SPI_SCLK	I/O	SPI clock input/output
50	GPIO43	I/O	General-purpose input/output 43
	I2C_SDA	I/O	I^2C data
	COMP6L	O	Comparator COMP6L result output
	SPI_SFRM	I/O	SPI frame signal
51	GPIO44	I/O	General-purpose input/output 44
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	COMP7H	O	Comparator COMP7H result output
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
52	GPIO45	I/O	General-purpose input/output 45
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data

Pin	Signal	Type[1]	Description
	COMP7L	O	Comparator COMP7L result output
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
53	BOOT(GPIO47)	I/O	Boot pin (General-purpose input/output 47)
54	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
55	DVSS	S	Digital ground
56	VCAP12	S	1.2V power, add 0.1uF bypass ceramic cap to DVSS
57	XRSTn	I	Device reset pin, reset the device when low
58	TRSTn	I	JTAG reset pin, reset the JTAG when low
59	GPIO48	I/O	General-purpose input/output 48
	TCK/SWCK	I	JTAG clock or SWD clock
	COMP0H	O	Comparator COMP0H result output
	COMP3H	O	Comparator COMP3H result output
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
60	GPIO49	I/O	General-purpose input/output 49
	TMS/SWD	I/O	JTAG mode select or SWD data
	COMP0L	O	Comparator COMP0L result output
	COMP3L	O	Comparator COMP3L result output
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
61	GPIO50	I/O	General-purpose input/output 50
	TDI	I	JTAG data input
	SWCK(CAU)	I	SWD clock for CAU
	COMP1H	O	Comparator COMP1H result output
	COMP4H	O	Comparator COMP4H result output
	Note: when TRSTn is HIGH, this pin always works as TDI or SWCK(CAU) and can't be configured as other functions.		
62	GPIO51	I/O	General-purpose input/output 51
	TDO	O	JTAG data output
	SWD(CAU)	I/O	SWD data for CAU
	COMP1L	O	Comparator COMP1L result output
	COMP4L	O	Comparator COMP4L result output
	Note: when TRSTn is HIGH, this pin always works as TDO or SWD(CAU) and can't be configured as other functions.		
63	GPIO56	I/O	General-purpose input/output 56
	PWM4A	O	PWM4 output A
64	GPIO57	I/O	General-purpose input/output 57
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B

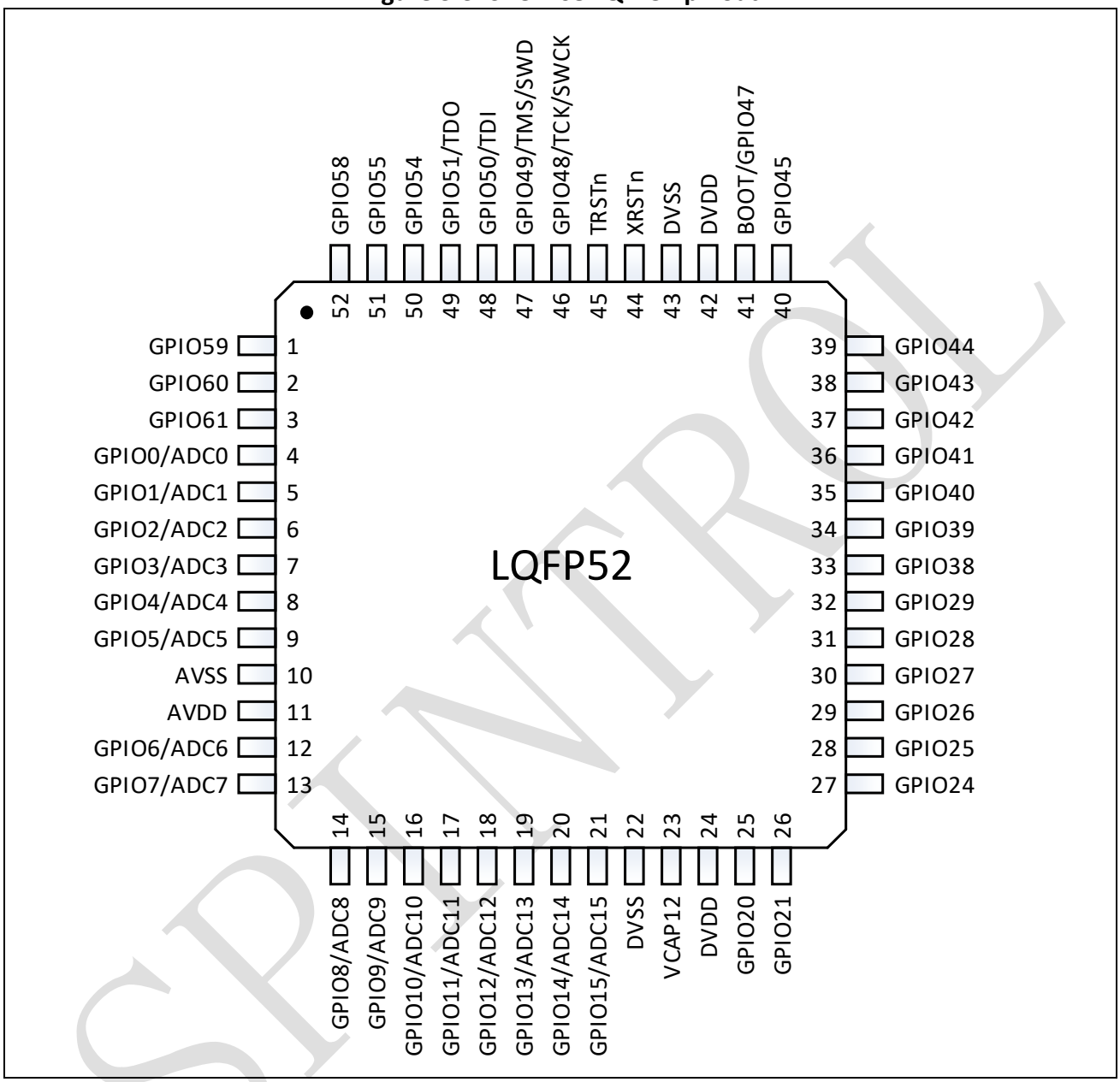
[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] PWMSOC signal is logic OR of PWMSOCA, PWMSOCB and PWMSOCC signal.

[3] All GPIO pins can be configured as ECAP input or output.

3.3 LQFP52

Figure 3-3: SPC2168 LQFP52 pinout



[1] The figure above shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO48 ~ GPIO51 pins work as Debug interface and can't be configured as other functions.

Table 3-3: SPC2168 LQFP52 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO59	I/O	General-purpose input/output 59
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
2	GPIO60	I/O	General-purpose input/output 60
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
3	GPIO61	I/O	General-purpose input/output 61
	PWM6B	O	PWM6 output B
4	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
5	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
6	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
7	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
8	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
9	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
10	AVSS	S	Analog ground
11	AVDD	S	Analog power, add 4.7uF and 0.1uF bypass ceramic cap to AVSS
12	GPIO6	I/O	General-purpose input/output 6
	ADC6	AI	ADC channel 6 input
13	GPIO7	I/O	General-purpose input/output 7
	ADC7	AI	ADC channel 7 input
14	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
15	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
16	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	COMP3H	O	Comparator COMP3H result output
17	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input

Pin	Signal	Type[1]	Description
	COMP3L	O	Comparator COMP3L result output
	DCLK	O	Clock output from CLKDET module for monitoring
18	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	COMP4H	O	Comparator COMP4H result output
19	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	COMP4L	O	Comparator COMP4L result output
20	GPIO14	I/O	General-purpose input/output 14
	ADC14	AI	ADC channel 14 input
	COMP5H	O	Comparator COMP5H result output
21	GPIO15	I/O	General-purpose input/output 15
	ADC15	AI	ADC channel 15 input
	COMP5L	O	Comparator COMP5L result output
22	DVSS	S	Digital ground
23	VCAP12	S	1.2V power, add 4.7uF bypass ceramic cap to DVSS
24	DVDD	S	Digital power, add 4.7uF and 0.1uF ceramic cap to DVSS
25	GPIO20	I/O	General-purpose input/output 20
	XIN	AI	External oscillator input
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	UART_TXD	O	UART transmit data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
26	GPIO21	I/O	General-purpose input/output 21
	XIO	AI/O	External oscillator input or output
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	UART_RXD	I	UART receive data
	PWMSOC[2]	O	PWM SOC signal output for monitoring
27	GPIO24	I/O	General-purpose input/output 24
	COMP0H	O	Comparator COMP0H result output
	PWM1A	O	PWM1 output A
28	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM2A	O	PWM2 output A
	PWM1B	O	PWM1 output B
29	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM3A	O	PWM3 output A
	PWM2A	O	PWM2 output A
30	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM1B	O	PWM1 output B

Pin	Signal	Type[1]	Description
	PWM2B	O	PWM2 output B
31	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM2B	O	PWM2 output B
	PWM3A	O	PWM3 output A
32	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM3B	O	PWM3 output B
33	GPIO38	I/O	General-purpose input/output 38
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWMSOCA	O	PWM SOCA signal output for monitoring
34	GPIO39	I/O	General-purpose input/output 39
	SPI_SFRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWMSOCB	O	PWM SOCB signal output for monitoring
35	GPIO40	I/O	General-purpose input/output 40
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I^2C clock
	PWMSOCC	O	PWM SOCC signal output for monitoring
36	GPIO41	I/O	General-purpose input/output 41
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I^2C data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
37	GPIO42	I/O	General-purpose input/output 42
	I2C_SCL	I/O	I^2C clock
	COMP6H	O	Comparator COMP6H result output
	SPI_SCLK	I/O	SPI clock input/output
38	GPIO43	I/O	General-purpose input/output 43
	I2C_SDA	I/O	I^2C data
	COMP6L	O	Comparator COMP6L result output
	SPI_SFRM	I/O	SPI frame signal
39	GPIO44	I/O	General-purpose input/output 44
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	COMP7H	O	Comparator COMP7H result output
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
40	GPIO45	I/O	General-purpose input/output 45

Pin	Signal	Type[1]	Description
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	COMP7L	O	Comparator COMP7L result output
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
41	BOOT(GPIO47)	I/O	Boot pin (General-purpose input/output 47)
42	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to DVSS
43	DVSS	S	Digital ground
44	XRSTn	I	Device reset pin, reset the device when low
45	TRSTn	I	JTAG reset pin, reset the JTAG when low
46	GPIO48	I/O	General-purpose input/output 48
	TCK/SWCK	I	JTAG clock or SWD clock
	COMP0H	O	Comparator COMP0H result output
	COMP3H	O	Comparator COMP3H result output
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
47	GPIO49	I/O	General-purpose input/output 49
	TMS/SWD	I/O	JTAG mode select or SWD data
	COMP0L	O	Comparator COMP0L result output
	COMP3L	O	Comparator COMP3L result output
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
48	GPIO50	I/O	General-purpose input/output 50
	TDI	I	JTAG data input
	SWCK(CAU)	I	SWD clock for CAU
	COMP1H	O	Comparator COMP1H result output
	COMP4H	O	Comparator COMP4H result output
	Note: when TRSTn is HIGH, this pin always works as TDI or SWCK(CAU) and can't be configured as other functions.		
49	GPIO51	I/O	General-purpose input/output 51
	TDO	O	JTAG data output
	SWD(CAU)	I/O	SWD data for CAU
	COMP1L	O	Comparator COMP1L result output
	COMP4L	O	Comparator COMP4L result output
	Note: when TRSTn is HIGH, this pin always works as TDO or SWD(CAU) and can't be configured as other functions.		
50	GPIO54	I/O	General-purpose input/output 54
	PWM7A	O	PWM7 output A
	PWM4A	O	PWM4 output A
51	GPIO55	I/O	General-purpose input/output 55
	PWM7B	O	PWM7 output B
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B

Pin	Signal	Type[1]	Description
52	GPIO58	I/O	General-purpose input/output 58
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A

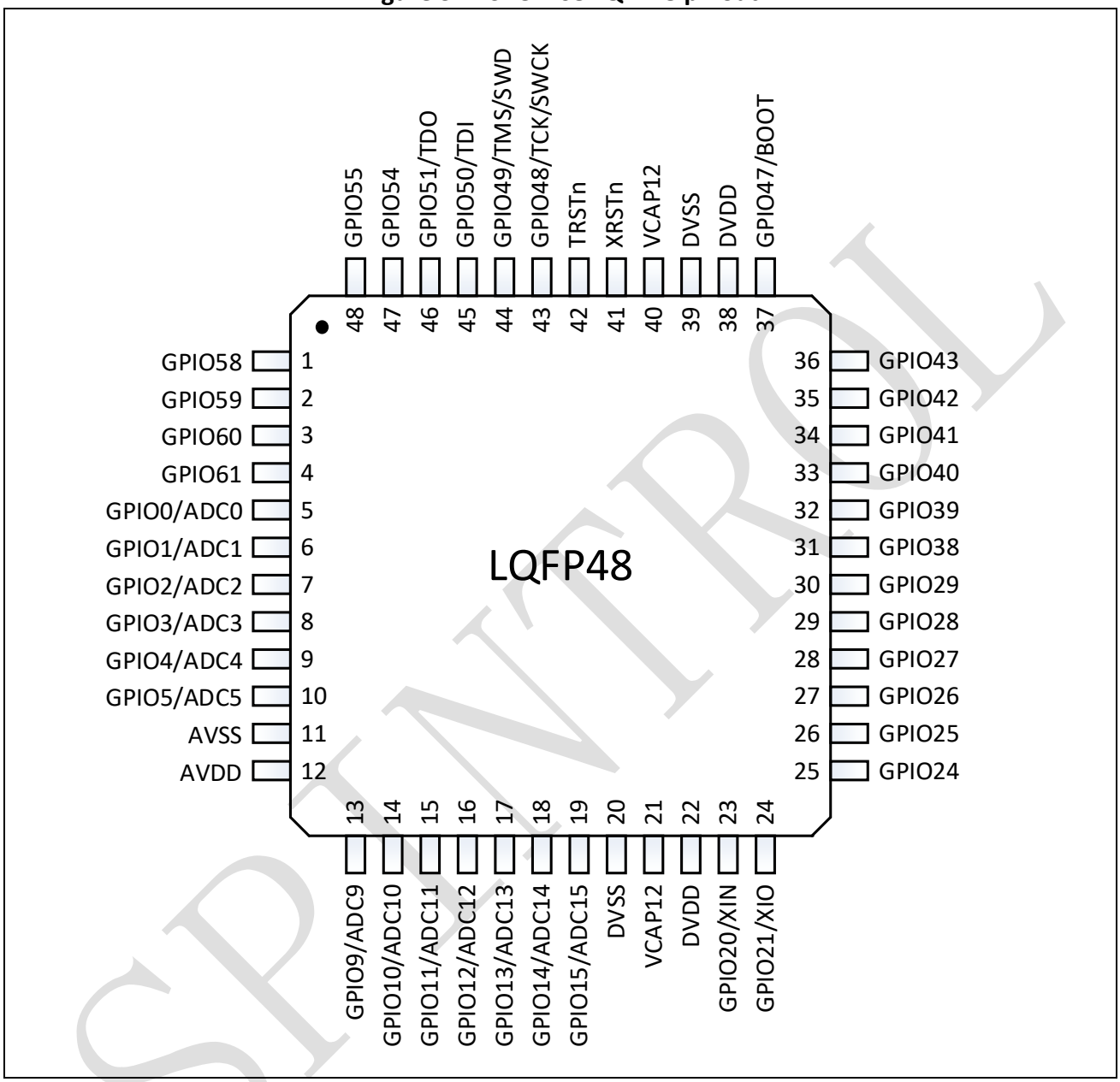
[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] PWMSOC signal is logic OR of PWMSOCA, PWMSOCB and PWMSOCC signal.

[3] All GPIO pins can be configured as ECAP input or output.

3.4 LQFP48

Figure 3-4: SPC2168 LQFP48 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO48 ~ GPIO51 pins work as Debug interface and can't be configured as other functions.

Table 3-4: SPC2168 LQFP48 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO58	I/O	General-purpose input/output 58
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
2	GPIO59	I/O	General-purpose input/output 59
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B
3	GPIO60	I/O	General-purpose input/output 60
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
4	GPIO61	I/O	General-purpose input/output 61
	PWM6B	O	PWM6 output B
5	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
6	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
7	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
8	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
9	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
10	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
11	AVSS	S	Analog ground
12	AVDD	S	Analog power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
13	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
14	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	COMP3H	O	Comparator COMP3H result output
15	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	COMP3L	O	Comparator COMP3L result output
	DCLK	O	Clock output from CLKDET module for monitoring
16	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input

Pin	Signal	Type[1]	Description
	COMP4H	O	Comparator COMP4H result output
17	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	COMP4L	O	Comparator COMP4L result output
18	GPIO14	I/O	General-purpose input/output 14
	ADC14	AI	ADC channel 14 input
	COMP5H	O	Comparator COMP5H result output
19	GPIO15	I/O	General-purpose input/output 15
	ADC15	AI	ADC channel 15 input
	COMP5L	O	Comparator COMP5L result output
20	DVSS	S	Digital ground
21	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
22	DVDD	S	Digital power, **add 4.7uF and 0.1uF ceramic cap to DVSS**
23	GPIO20	I/O	General-purpose input/output 20
	XIN	AI	External oscillator input
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	UART_TXD	O	UART transmit data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
24	GPIO21	I/O	General-purpose input/output 21
	XIO	AI/O	External oscillator input or output
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	UART_RXD	I	UART receive data
	PWMSOC[2]	O	PWM SOC signal output for monitoring
25	GPIO24	I/O	General-purpose input/output 24
	COMP0H	O	Comparator COMP0H result output
	PWM1A	O	PWM1 output A
26	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM2A	O	PWM2 output A
	PWM1B	O	PWM1 output B
27	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM3A	O	PWM3 output A
	PWM2A	O	PWM2 output A
28	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM1B	O	PWM1 output B
	PWM2B	O	PWM2 output B
29	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM2B	O	PWM2 output B

Pin	Signal	Type[1]	Description
	PWM3A	O	PWM3 output A
30	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM3B	O	PWM3 output B
31	GPIO38	I/O	General-purpose input/output 38
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWMSOCA	O	PWM SOCA signal output for monitoring
32	GPIO39	I/O	General-purpose input/output 39
	SPI_SFRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWMSOCB	O	PWM SOCB signal output for monitoring
33	GPIO40	I/O	General-purpose input/output 40
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I^2C clock
	PWMSOCC	O	PWM SOCC signal output for monitoring
34	GPIO41	I/O	General-purpose input/output 41
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I^2C data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
35	GPIO42	I/O	General-purpose input/output 42
	I2C_SCL	I/O	I^2C clock
	COMP6H	O	Comparator COMP6H result output
	SPI_SCLK	I/O	SPI clock input/output
36	GPIO43	I/O	General-purpose input/output 43
	I2C_SDA	I/O	I^2C data
	COMP6L	O	Comparator COMP6L result output
	SPI_SFRM	I/O	SPI frame signal
37	BOOT(GPIO47)	I/O	Boot pin (General-purpose input/output 47)
38	DVDD	S	Digital power, **add 0.1uF bypass ceramic cap to DVSS**
39	DVSS	S	Digital ground
40	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
41	XRSTn	I	Device reset pin, reset the device when low
42	TRSTn	I	JTAG reset pin, reset the JTAG when low
43	GPIO48	I/O	General-purpose input/output 48
	TCK/SWCK	I	JTAG clock or SWD clock
	COMP0H	O	Comparator COMP0H result output
	COMP3H	O	Comparator COMP3H result output
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as		

Pin	Signal	Type[1]	Description
	other functions.		
44	GPIO49	I/O	General-purpose input/output 49
	TMS/SWD	I/O	JTAG mode select or SWD data
	COMP0L	O	Comparator COMP0L result output
	COMP3L	O	Comparator COMP3L result output
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
45	GPIO50	I/O	General-purpose input/output 50
	TDI	I	JTAG data input
	SWCK(CAU)	I	SWD clock for CAU
	COMP1H	O	Comparator COMP1H result output
	COMP4H	O	Comparator COMP4H result output
	Note: when TRSTn is HIGH, this pin always works as TDI or SWCK(CAU) and can't be configured as other functions.		
46	GPIO51	I/O	General-purpose input/output 51
	TDO	O	JTAG data output
	SWD(CAU)	I/O	SWD data for CAU
	COMP1L	O	Comparator COMP1L result output
	COMP4L	O	Comparator COMP4L result output
	Note: when TRSTn is HIGH, this pin always works as TDO or SWD(CAU) and can't be configured as other functions.		
47	GPIO54	I/O	General-purpose input/output 54
	PWM7A	O	PWM7 output A
	PWM4A	O	PWM4 output A
48	GPIO55	I/O	General-purpose input/output 55
	PWM7B	O	PWM7 output B
	PWM5A	O	PWM5 output A
	PWM4B	O	PWM4 output B

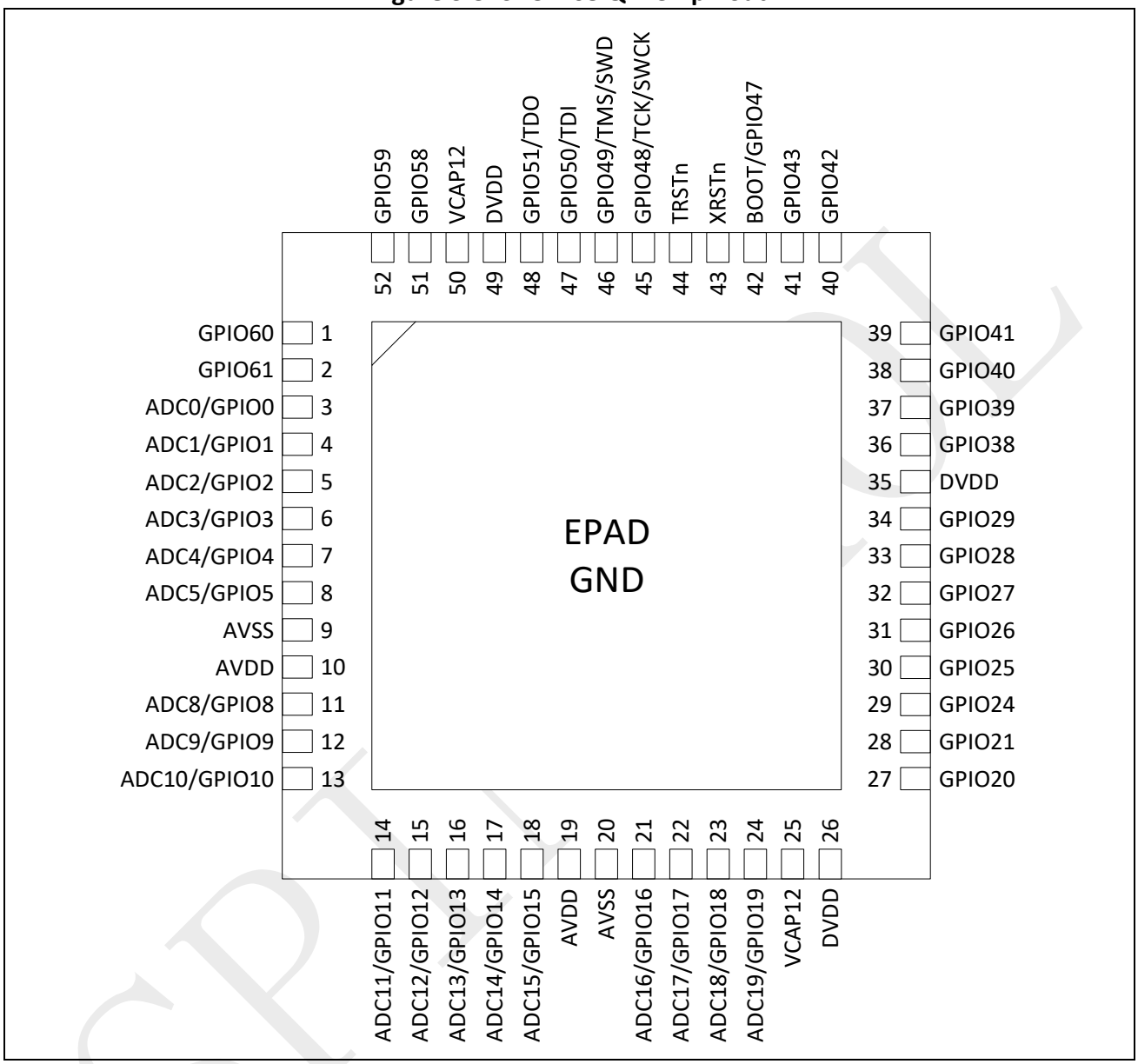
[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] PWMSOC signal is logic OR of PWMSOCA, PWMSOCB and PWMSOCC signal.

[3] All GPIO pins can be configured as ECAP input or output.

3.5 QFN52

Figure 3-5: SPC2168 QFN52 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO48 ~ GPIO51 pins work as Debug interface and can't be configured as other functions.

Table 3-5: SPC2168 QFN52 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO60	I/O	General-purpose input/output 60
	PWM5B	O	PWM5 output B
	PWM6A	O	PWM6 output A
2	GPIO61	I/O	General-purpose input/output 61
	PWM6B	O	PWM6 output B
3	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
4	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
5	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
6	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
7	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
8	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
9	AVSS	S	Analog ground
10	AVDD	S	Analog power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
11	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
12	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
13	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	COMP3H	O	Comparator COMP3H result output
14	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	COMP3L	O	Comparator COMP3L result output
	DCLK	O	Clock output from CLKDET module for monitoring
15	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	COMP4H	O	Comparator COMP4H result output
16	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	COMP4L	O	Comparator COMP4L result output

Pin	Signal	Type[1]	Description
17	GPIO14	I/O	General-purpose input/output 14
	ADC14	AI	ADC channel 14 input
	COMP5H	O	Comparator COMP5H result output
18	GPIO15	I/O	General-purpose input/output 15
	ADC15	AI	ADC channel 15 input
	COMP5L	O	Comparator COMP5L result output
19	AVDD	S	Analog power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
20	AVSS	S	Analog ground
21	GPIO16	I/O	General-purpose input/output 16
	ADC16	AI	ADC channel 16 input
	COMP6H	O	Comparator COMP6H result output
22	GPIO17	I/O	General-purpose input/output 17
	ADC17	AI	ADC channel 17 input
	COMP6L	O	Comparator COMP6L result output
23	GPIO18	I/O	General-purpose input/output 18
	ADC18	AI	ADC channel 18 input
	COMP7H	O	Comparator COMP7H result output
24	GPIO19	I/O	General-purpose input/output 19
	ADC19	AI	ADC channel 19 input
	COMP7L	O	Comparator COMP7L result output
25	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
26	DVDD	S	Digital power, **add 4.7uF and 0.1uF ceramic cap to DVSS**
27	GPIO20	I/O	General-purpose input/output 20
	XIN	AI	External oscillator input
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	UART_TXD	O	UART transmit data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
28	GPIO21	I/O	General-purpose input/output 21
	XIO	AI/O	External oscillator input or output
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	UART_RXD	I	UART receive data
	PWMSOC[2]	O	PWM SOC signal output for monitoring
29	GPIO24	I/O	General-purpose input/output 24
	COMP0H	O	Comparator COMP0H result output
	PWM1A	O	PWM1 output A
30	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM2A	O	PWM2 output A
	PWM1B	O	PWM1 output B
31	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output

Pin	Signal	Type[1]	Description
	PWM3A	O	PWM3 output A
	PWM2A	O	PWM2 output A
32	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM1B	O	PWM1 output B
	PWM2B	O	PWM2 output B
33	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM2B	O	PWM2 output B
	PWM3A	O	PWM3 output A
34	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM3B	O	PWM3 output B
35	DVDD	S	Digital power, **add 0.1uF bypass ceramic cap to DVSS**
36	GPIO38	I/O	General-purpose input/output 38
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWMSOCA	O	PWM SOCA signal output for monitoring
37	GPIO39	I/O	General-purpose input/output 39
	SPI_SFRM	I/O	SPI frame signal
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWMSOCB	O	PWM SOCB signal output for monitoring
38	GPIO40	I/O	General-purpose input/output 40
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I^2C clock
	PWMSOCC	O	PWM SOCC signal output for monitoring
39	GPIO41	I/O	General-purpose input/output 41
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I^2C data
	PWMSYNCO	O	PWMSYNCO signal output for monitoring
40	GPIO42	I/O	General-purpose input/output 42
	I2C_SCL	I/O	I^2C clock
	COMP6H	O	Comparator COMP6H result output
	SPI_SCLK	I/O	SPI clock input/output
41	GPIO43	I/O	General-purpose input/output 43
	I2C_SDA	I/O	I^2C data
	COMP6L	O	Comparator COMP6L result output
	SPI_SFRM	I/O	SPI frame signal
42	BOOT(GPIO47)	I/O	Boot pin (General-purpose input/output 47)

Pin	Signal	Type[1]	Description
43	XRSTn	I	Device reset pin, reset the device when low
44	TRSTn	I	JTAG reset pin, reset the JTAG when low
45	GPIO48	I/O	General-purpose input/output 48
	TCK/SWCK	I	JTAG clock or SWD clock
	COMP0H	O	Comparator COMP0H result output
	COMP3H	O	Comparator COMP3H result output
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
46	GPIO49	I/O	General-purpose input/output 49
	TMS/SWD	I/O	JTAG mode select or SWD data
	COMP0L	O	Comparator COMP0L result output
	COMP3L	O	Comparator COMP3L result output
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
47	GPIO50	I/O	General-purpose input/output 50
	TDI	I	JTAG data input
	SWCK(CAU)	I	SWD clock for CAU
	COMP1H	O	Comparator COMP1H result output
	COMP4H	O	Comparator COMP4H result output
	Note: when TRSTn is HIGH, this pin always works as TDI or SWCK(CAU) and can't be configured as other functions.		
48	GPIO51	I/O	General-purpose input/output 51
	TDO	O	JTAG data output
	SWD(CAU)	I/O	SWD data for CAU
	COMP1L	O	Comparator COMP1L result output
	COMP4L	O	Comparator COMP4L result output
	Note: when TRSTn is HIGH, this pin always works as TDO or SWD(CAU) and can't be configured as other functions.		
49	DVDD	S	Digital power, **add 0.1uF bypass ceramic cap to DVSS**
50	VCAP12	S	1.2V power, **add 0.1uF bypass ceramic cap to DVSS**
51	GPIO58	I/O	General-purpose input/output 58
	PWM6A	O	PWM6 output A
	PWM5A	O	PWM5 output A
52	GPIO59	I/O	General-purpose input/output 59
	PWM4B	O	PWM4 output B
	PWM5B	O	PWM5 output B

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] PWMSOC signal is logic OR of PWMSOCA, PWMSOCB and PWMSOCC signal.

[3] All GPIO pins can be configured as ECAP input or output.

3.6 PGA input channel selection

For the six on-MCU PGA's, each PGA has two 1-of-8 multiplexers (MUX) for input channel selection, one is for positive input (PGAx_P, x = 0~5) and the other is for negative input (PGAx_N, x = 0~5). The input channel selection table is shown below.

Table 3-6: PGA0/1/2 input channel selection

MUX Value	PGA0_P	PGA0_N	PGA1_P	PGA1_N	PGA2_P	PGA2_N
0	GND	GND	GND	GND	GND	GND
1	DAC0	DAC0	DAC0	DAC0	DAC0	DAC0
2	DAC2	DAC3	ATEST	VREF12	ADC10	VDD12
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
4	ADC2	ADC3	ADC2	ADC3	ADC2	ADC1
5	ADC4	ADC5	ADC4	ADC5	ADC4	ADC5
6	ADC6	ADC7	ADC6	ADC7	ADC6	ADC7
7	ADC8	ADC9	ADC8	ADC9	ADC8	ADC9

Table 3-7: PGA3/4/5 input channel selection

MUX Value	PGA3_P	PGA3_N	PGA4_P	PGA4_N	PGA5_P	PGA5_N
0	GND	GND	GND	GND	GND	GND
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
2	DAC4	DAC5	ADC11	ADC0	TSEN1	TSEN0
3	ADC10	ADC11	ADC10	ADC12	ADC10	ADC13
4	ADC12	ADC13	ADC12	ADC13	ADC12	ADC11
5	ADC14	ADC15	ADC14	ADC15	ADC14	ADC15
6	ADC16	ADC17	ADC16	ADC17	ADC16	ADC17
7	ADC18	ADC19	ADC18	ADC19	ADC18	ADC19

[1] TSEN0 is output 0 of T-Sensor and TSEN1 is output 1 of T-Sensor.

3.7 GPIO pin function and state after reset

Table 3-8: GPIO pin function and state after reset

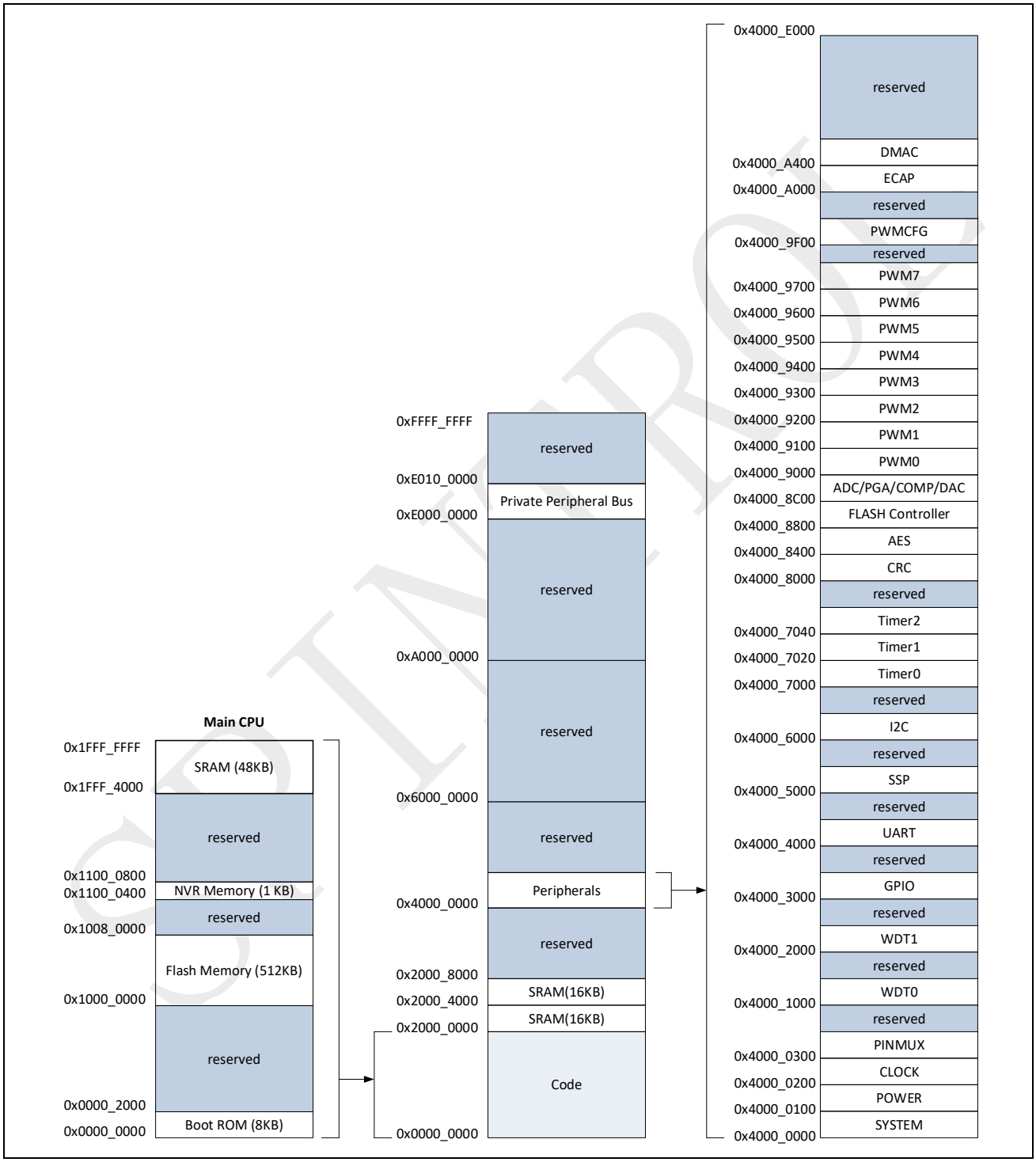
Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
GPIO4	ADC4	Floating
GPIO5	ADC5	Floating
GPIO6	ADC6	Floating
GPIO7	ADC7	Floating
GPIO8	ADC8	Floating
GPIO9	ADC9	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO12	ADC12	Floating
GPIO13	ADC13	Floating
GPIO14	ADC14	Floating
GPIO15	ADC15	Floating
GPIO16	ADC16	Floating
GPIO17	ADC17	Floating
GPIO18	ADC18	Floating
GPIO19	ADC19	Floating
GPIO20	GPIO20	Pull up
GPIO21	GPIO21	Pull up
GPIO22	GPIO22	Pull up
GPIO23	GPIO23	Pull up
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Floating
GPIO26	GPIO26	Floating
GPIO27	GPIO27	Floating
GPIO28	GPIO28	Floating
GPIO29	GPIO29	Floating
GPIO30	GPIO30	Pull up
GPIO31	GPIO31	Pull up
GPIO32	GPIO32	Floating
GPIO33	GPIO33	Floating
GPIO34	GPIO34	Floating
GPIO35	GPIO35	Floating
GPIO36	GPIO36	Floating
GPIO37	GPIO37	Floating
GPIO38	GPIO38	Pull up
GPIO39	GPIO39	Pull up

Pin Name	Default Function	Default State
GPIO40	GPIO40	Pull up
GPIO41	GPIO41	Pull up
GPIO42	GPIO42	Pull up
GPIO43	GPIO43	Pull up
GPIO44	GPIO44	Pull up
GPIO45	GPIO45	Pull up
GPIO46	GPIO46	Pull up
GPIO47	GPIO47	Pull up
GPIO48	GPIO48	Pull up
GPIO49	GPIO49	Pull up
GPIO50	GPIO50	Pull up
GPIO51	GPIO51	Pull up
GPIO52	GPIO52	Floating
GPIO53	GPIO53	Floating
GPIO54	GPIO54	Floating
GPIO55	GPIO55	Floating
GPIO56	GPIO56	Floating
GPIO57	GPIO57	Floating
GPIO58	GPIO58	Floating
GPIO59	GPIO59	Floating
GPIO60	GPIO60	Floating
GPIO61	GPIO61	Floating

4 Memory mapping

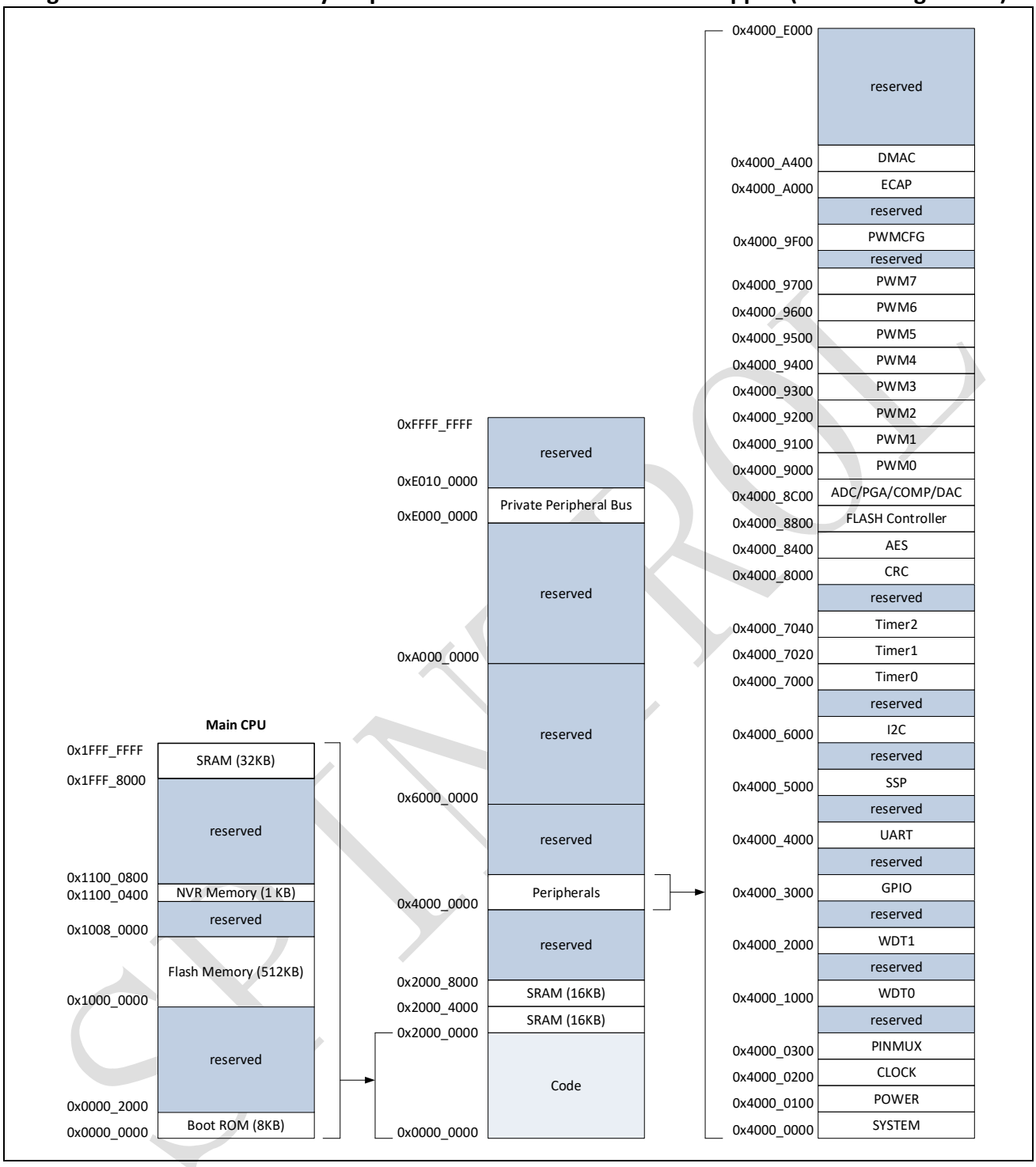
The memory map of SPC2168 is shown in Figure 4-1 to Figure 4-4.

Figure 4-1: SPC2168 memory map with Cache disabled and CAU stopped (Used as single-core)



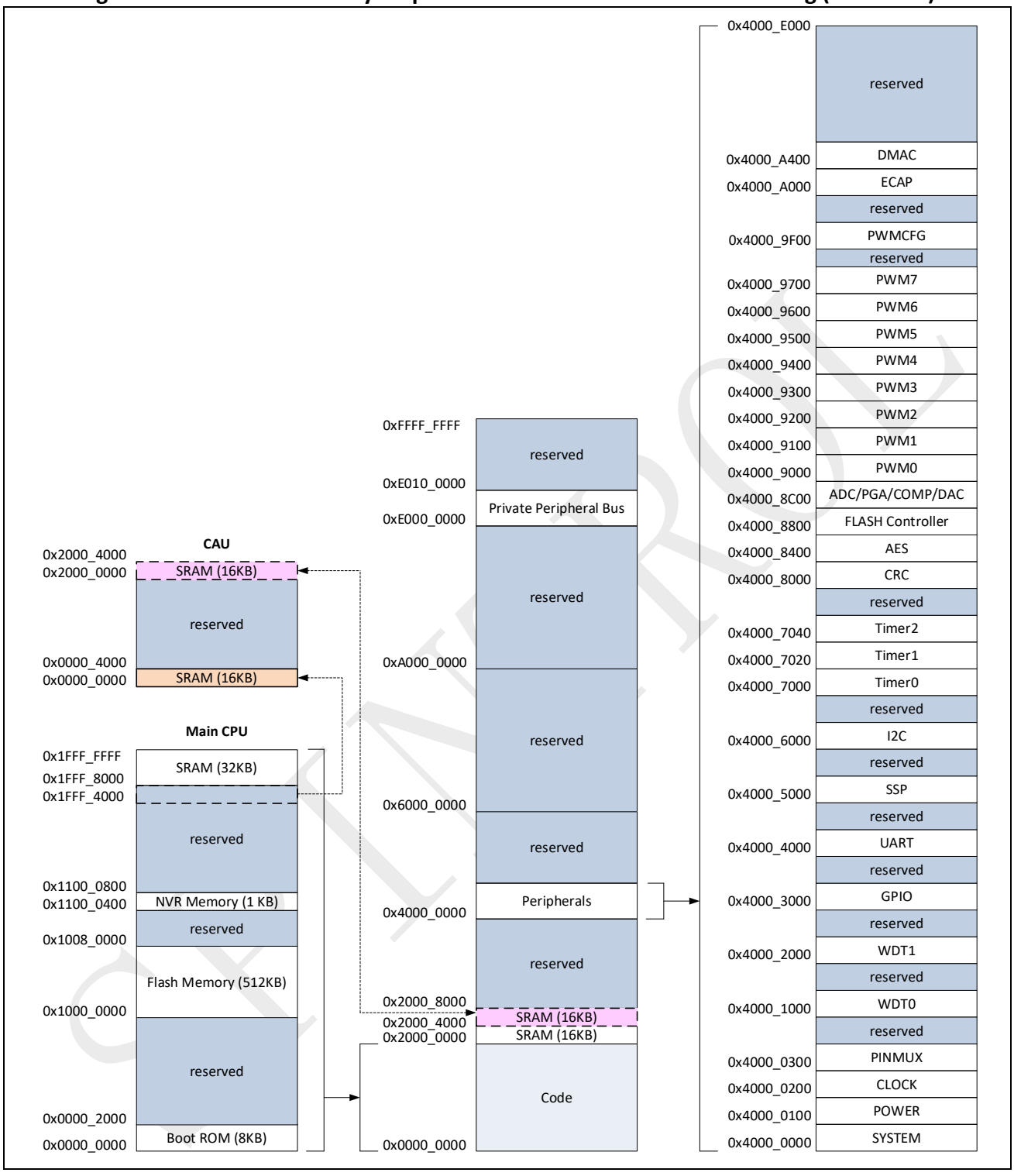
With the XIP cache disabled and the CAU disabled, the entire 80 KB can be accessed by the Main CPU at addresses 0x1FFF4000 to 0x20007FFF.

Figure 4-2: SPC2168 memory map with Cache enabled and CAU stopped (Used as single-core)



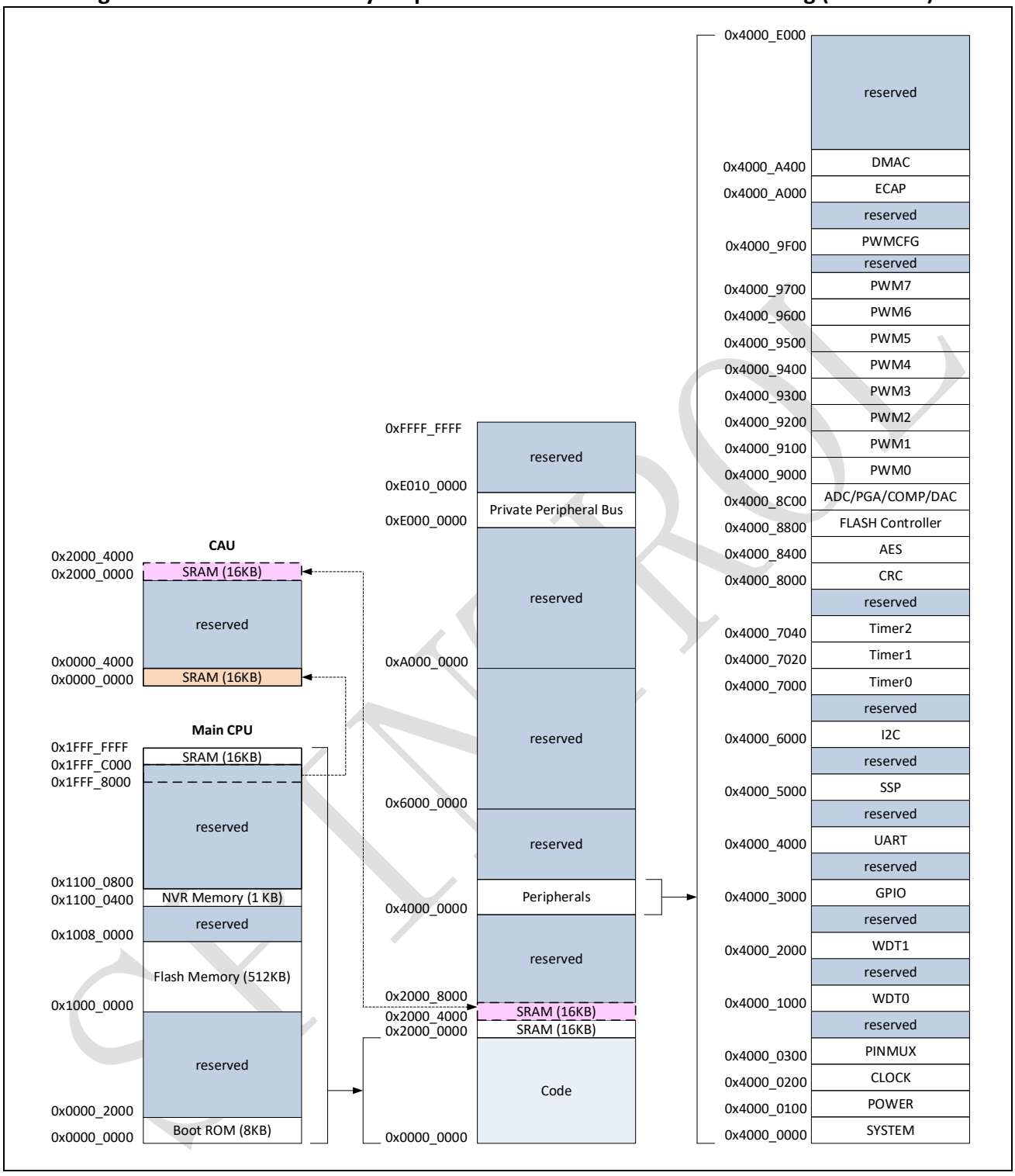
With the XIP cache enabled and the CAU disabled, 16 KB of SRAM is used as the XIP cache. The remaining 64 KB is allocated to the Main CPU, accessible at addresses 0x1FFF8000 to 0x20007FFF

Figure 4-3: SPC2168 memory map with Cache disabled and CAU running (Dual core)



With the XIP cache disabled and the CAU enabled, 48 KB of SRAM is allocated to the Main CPU, accessible at address 0x1FFF8000 ~ 0x20003FFF. Another 16 KB of SRAM can be accessed by both the Main CPU (at 0x20004000 ~ 0x20007FFF) and the CAU (at 0x20000000 ~ 0x20003FFF). The remaining 16 KB of SRAM, which was originally accessible to the Main CPU at address 0x1FFF4000 ~ 0x1FFF7FFF for initializing CAU code, is now allocated to the CAU as code RAM, accessible by the CAU at address 0x0000 ~ 0x3FFF.

Figure 4-4: SPC2168 memory map with Cache enabled and CAU running (Dual core)



With the XIP cache enabled and the CAU enabled, 16 KB of SRAM is used as the XIP cache. 32 KB of SRAM is allocated to the Main CPU, accessible at address 0x1FFFC000 ~ 0x20003FFF. Another 16 KB of SRAM can be accessed by both the Main CPU (at 0x20004000 ~ 0x20007FFF) and the CAU (at 0x20000000 ~ 0x20003FFF). The remaining 16 KB of SRAM, which was originally accessible to the Main CPU at address 0x1FFF8000 ~ 0x1FFFBFFF for initializing CAU code, is now allocated to the CAU as code RAM, accessible by the CAU at address 0x0000 ~ 0x3FFF.

5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings(1)(2)

Symbol	Parameter	Min	Max	Unit
V_{VDD}	Supply voltage, with respect to V_{VSS}	-0.3	4.6	V
V_{VDDA}	Analog voltage, with respect to V_{VSSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{VDD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_A	Ambient temperature(3)	-40	+105	°C
T_{stg}	Storage temperature(3)	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to V_{VSS}, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{VDD}	Supply voltage	–	2.97	3.3	3.63	V
V_{VSS}	Supply ground	–	–	0	–	V
V_{VDDA}	Analog supply voltage	–	2.97	3.3	3.63	V
V_{VCAP12}	Output voltage	–	1.08	1.20	1.32	V
V_{VSSA}	Analog ground	–	–	0	–	V
V_{IH}	High-level input voltage	V_{VDD} = 3.3 V	2.0	–	V_{VDD}+0.3	V
V_{IL}	Low-level input voltage	V_{VDD} = 3.3 V	V_{VSS} - 0.3	–	0.8	V
T_J	Junction temperature	–	-40	–	+125	°C
T_A	Ambient temperature	–	-40	–	+105	°C

5.3 I/O Electrical characteristics

Table 5-3: I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{VDD} - 0.4	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	–	–	0.4	V
V_{IH}	High-level input voltage	V_{VDD} = 3.3 V	2.0	–	V_{VDD} + 0.3	V
V_{IL}	Low-level input voltage	V_{VDD} = 3.3 V	V_{VSS} - 0.3	–	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{VDD} = 3.3V, V_{IH} = 0 V	–	–	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{VDD} = 3.3V, V_{IH} = V_{VDD}	–	–	2	uA
$\sum I_{OH}$	Total source current per I/O group [1]	–	–	–	80	mA
$\sum I_{OL}$	Total sink current per I/O group [1]	–	–	–	80	mA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	41	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{VDD}	–	42	–	kΩ

[1] The I/Os between two adjacent 3.3V power supply pins form a group.

5.4 Power consumption summary

Typical current consumption

In operational mode, the SPC2168 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is 1), except SSP (Max 50 MHz) I2C (Max 50 MHz), PCLK (Max 50 MHz) and DGCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.

In idle mode, the SPC2168 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO1 and XO) are disabled;
- Select RCO0 as system clock source with low-frequency mode enabled.

In deep sleep mode, the SPC2168 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO1 and XO) are disabled;
- 1.2V LDO is shut down to 0V.

The typical current consumption of SPC2168 measured from V_{VDD} is shown in Table 5-4 and Table 5-5. The operational current consumption over various HCLK frequency is shown in Figure 5-1.

Table 5-4: SPC2168 typical current consumption (Run in FLASH)

Mode	Conditions			-40°C	25 °C	125°C	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}				
Operational	200 MHz[2]	50 MHz	200 MHz	114.35	136.71	160.43	mA
	175 MHz[2]	43.75 MHz	175 MHz	102.02	126.86	150.96	mA
	168 MHz[2]	42 MHz	168 MHz	100.01	124.02	147.59	mA
	150 MHz[2]	50 MHz	150 MHz	93.624	117.24	142.93	mA
	125 MHz[2]	41.67 MHz	125 MHz	83.743	107.54	131.23	mA
	100 MHz	50 MHz	100 MHz	76.192	97.895	120.52	mA
	75 MHz	37.5 MHz	75 MHz	66.135	88.168	110.21	mA
	50 MHz	50 MHz	50 MHz	57.331	78.785	99.493	mA
	32 MHz	32 MHz	32 MHz	50.233	71.735	92.334	mA
	25 MHz	25 MHz	25 MHz	48.797	68.729	88.642	mA
Idle	110 Hz	110 Hz	–	6.7231	9.6037	13.484	mA
Sleep	–	–	–	10	10	10	uA

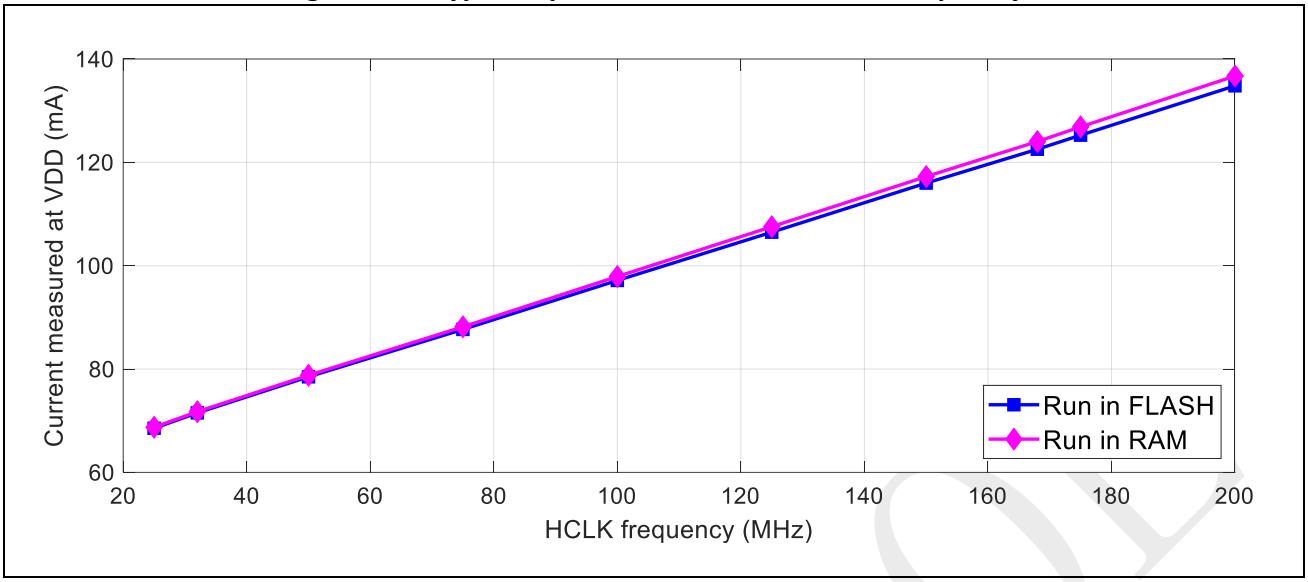
[1] Measured at V_{VDD} = 3.3 V.

Table 5-5: SPC2168 typical current consumption (Run in RAM)

Mode	Conditions			-40 °C	25 °C	125 °C	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}				
Operational	200 MHz[2]	50 MHz	200 MHz	113.45	134.80	159.24	mA
	175 MHz[2]	43.75 MHz	175 MHz	100.95	125.25	149.77	mA
	168 MHz[2]	42 MHz	168 MHz	98.743	122.53	146.23	mA
	150 MHz[2]	50 MHz	150 MHz	92.433	115.98	140.84	mA
	125 MHz[2]	41.67 MHz	125 MHz	82.558	106.47	130.01	mA
	100 MHz	50 MHz	100 MHz	74.996	97.137	119.02	mA
	75 MHz	37.5 MHz	75 MHz	64.932	87.666	108.98	mA
	50 MHz	50 MHz	50 MHz	56.001	78.487	98.102	mA
	32 MHz	32 MHz	32 MHz	48.983	71.509	91.019	mA
	25 MHz	25 MHz	25 MHz	47.522	68.530	87.333	mA
Idle	110 Hz	110 Hz	–	6.6432	9.5224	13.421	mA

[1] Measured at V_{VDD} = 3.3 V.

Figure 5-1: Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-6. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

Table 5-6: Peripheral current consumption

Peripherals[1]		Conditions	-40 °C	25 °C	125 °C	Unit
BOD		Select RCO0 as system clock source; All other peripherals use default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	0.1	0.1	0.1	mA
ADC	Analog[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 128 MHz, f_{PCLK} = 32 MHz, f_{PLL} = 128 MHz	15.99	16.52	17.05	mA
	Digital		2.12	2.31	2.55	mA
T-Sensor			0.16	0.16	0.16	mA
PGA[4]			4.10	4.10	4.10	mA
DAC			0.18	0.18	0.18	mA
Comparator			0.08	0.08	0.08	mA
CAU		200 MHz HCLK	6.001	6.263	6.612	mA
UART		UART clock 200 MHz, 256000 bps	0.416	0.456	0.901	mA
I2C		I2C clock 50 MHz, 2Mbps	0.288	0.312	0.344	mA
SSP		SSP clock 50 MHz, 50Mbps	0.321	0.356	0.391	mA
PWM		PWM clock 200 MHz	1.065	1.184	1.314	mA
ECAP		ECAP clock 200 MHz	0.349	0.360	0.372	mA

Peripherals[1]	Conditions	-40 °C	25 °C	125 °C	Unit
WDT	WDT clock 200 MHz	0.187	0.235	0.286	mA
TMR	TMR clock 200 MHz	0.301	0.337	0.374	mA
FLASH	HCLK clock 200 MHz	0.662	0.716	0.771	mA
XO	Use RCO0 as input for 200 MHz PLL	0.561	0.624	0.681	mA
RCO0	Use XO as input for 200 MHz PLL	0.145	0.157	0.169	mA
RCO1	Use XO as input for 200 MHz PLL	0.108	0.114	0.121	mA
PLL	XO as HCLK source, f_{PLL} = 32 MHz	1.812	1.961	2.132	mA

[1] For peripherals with multiple instances, the current quoted is for single modules. For example, the 4.10 mA value quoted for PGA is for one PGA module. So the total 3 PGA module current is 12.30mA.

[2] Values are measured at V_{VDD} = 3.3 V.

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.5 Internal 1.2V regulator characteristics

Table 5-7: Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDD}	Power supply	–	2.97	3.3	3.63	V
V_{VCAP12}	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔV_{VCAP12}	Load regulation	V_{VCAP12}(50mA load) - V_{VCAP12}(200mA load)	–	–	30	mV

Figure 5-2: Internal 1.2V regulator load regulation (T_A = 25 °C)

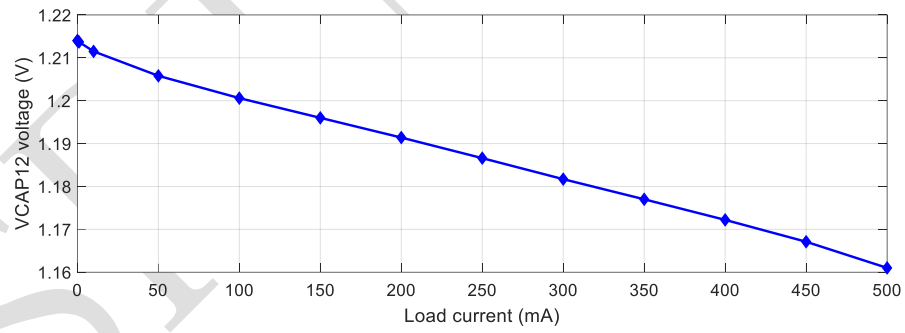
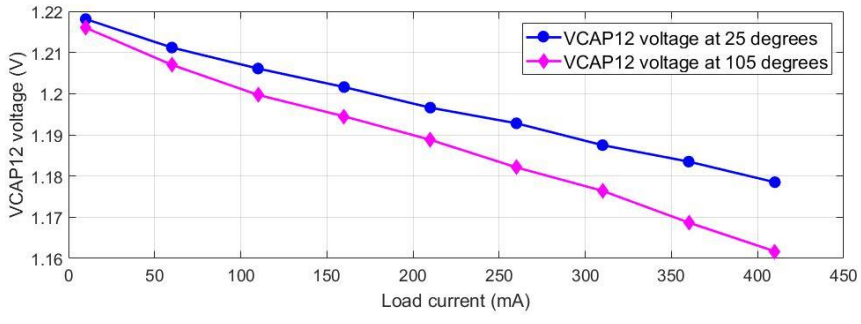


Figure 5-3: Internal 1.2V regulator load regulation with different temperature



5.6 BOD characteristics

Table 5-8: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
V_{VDD33H_Asset}	VDD33 too high assert threshold	–	–	3.42	–	V
$V_{VDD33H\_Deasset}$	VDD33 too high de-assert threshold	–	–	3.31	–	V
V_{VDD33L_Asset}	VDD33 too low assert threshold	–	–	2.58	–	V
$V_{VDD33L\_Deasset}$	VDD33 too low de-assert threshold	–	–	2.65	–	V
V_{VDD12H_Asset}	VDD12 too high assert threshold	–	–	1.33	–	V
$V_{VDD12H\_Deasset}$	VDD12 too high de-assert threshold	–	–	1.31	–	V
V_{VDD12L_Asset}	VDD12 too low assert threshold[1]	–	–	0.94	–	V
$V_{VDD12L\_Deasset}$	VDD12 too low de-assert threshold[1]	–	–	0.97	–	V

[1] The characteristics of VDD12 too low 0 and VDD12 too low 1 are the same.

5.7 RCO characteristics

Table 5-9: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
f_{RCO}	RCO frequency at room temperature	T_J = 25 °C	–	32	–	MHz
ACC_{RCO}	f_{RCO} accuracy (RCO frequency variation versus temperature)	T_J = -40~125 °C	-1	–	1	%

5.8 PLL characteristics

Table 5-10: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
f_{VCO}	VCO frequency	–	400	500	600	MHz
f_{pfd}	Phase-Frequency Detector (PFD) input frequency	–	4	–	8	MHz
t_{LOCK}	Locking time	–	–	–	15	us

5.9 XO characteristics

Table 5-11: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
f_{XO}	XO frequency	–	1	–	66	MHz

The negative resistance of the on-chip crystal oscillator at different temperature is shown in Figure 5-4 ~ Figure 5-7. The loading capacitor CL_eff is defined as equivalent capacitance seen by the on-chip crystal.

Figure 5-4: The negative resistance of the on-chip crystal oscillator at 50℃

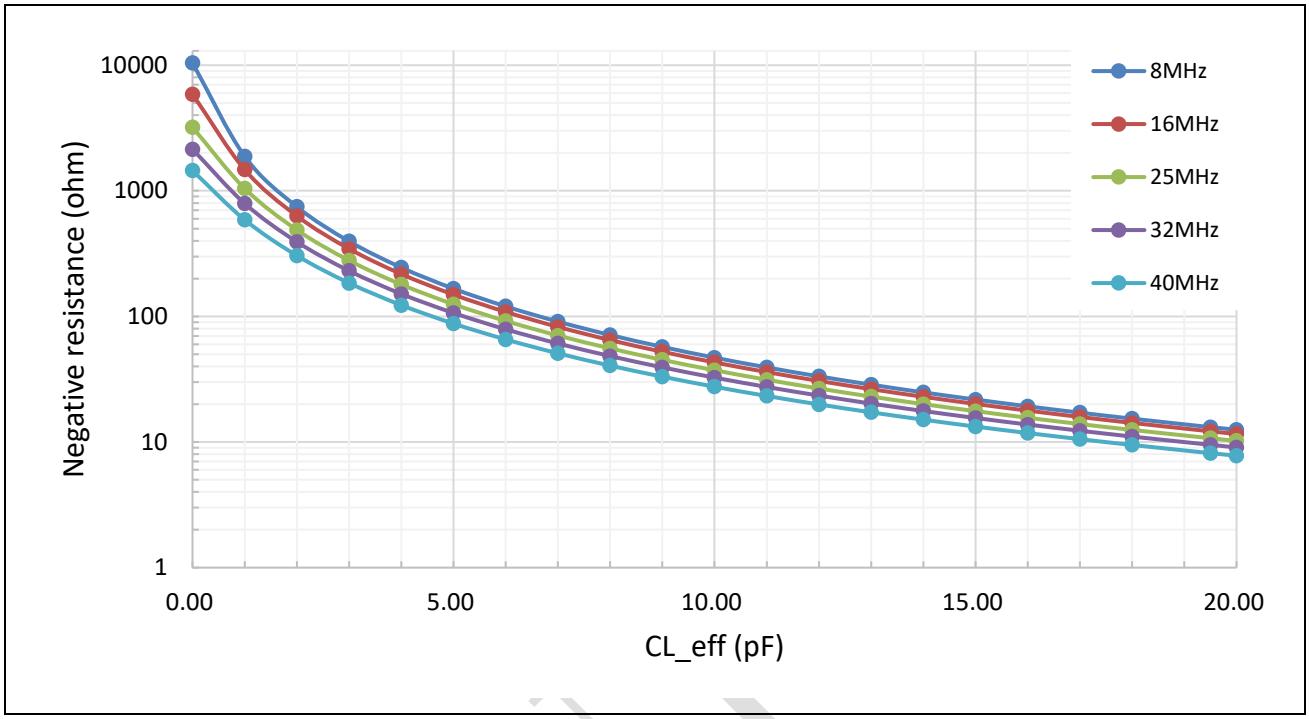


Figure 5-5: The negative resistance of the on-chip crystal oscillator at 85℃

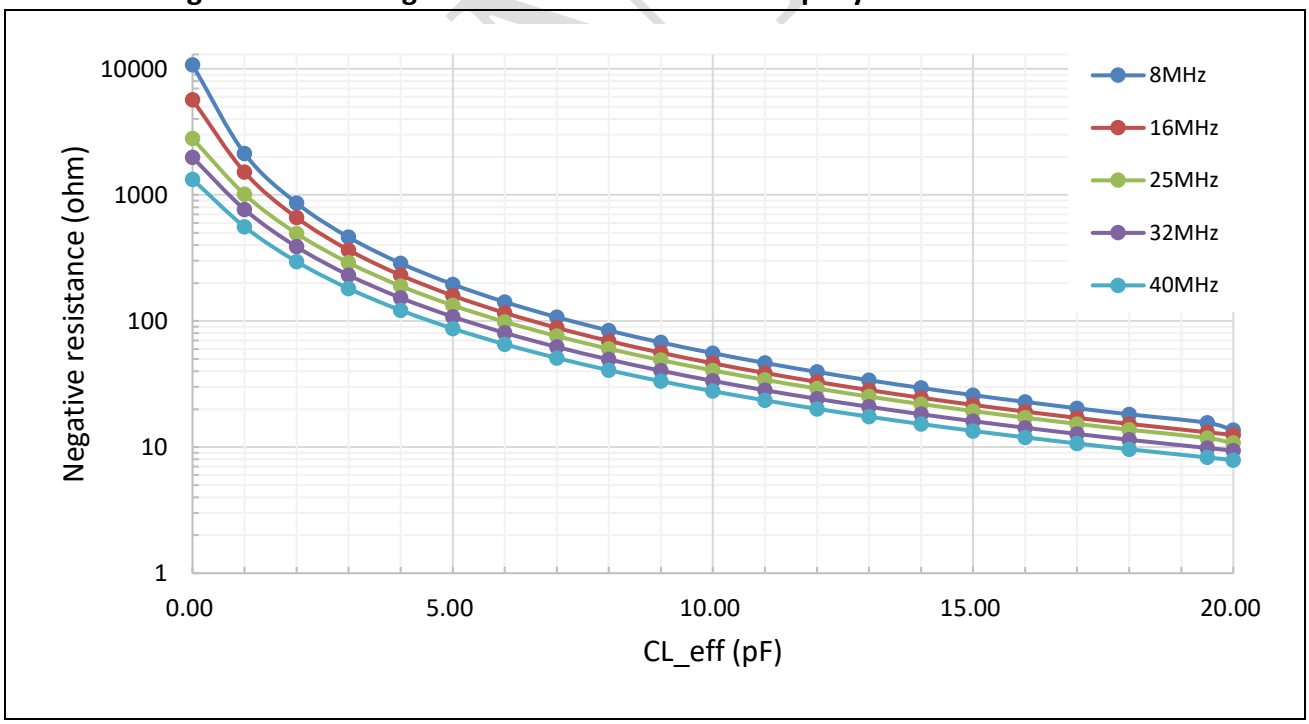


Figure 5-6: The negative resistance of the on-chip crystal oscillator at 100℃

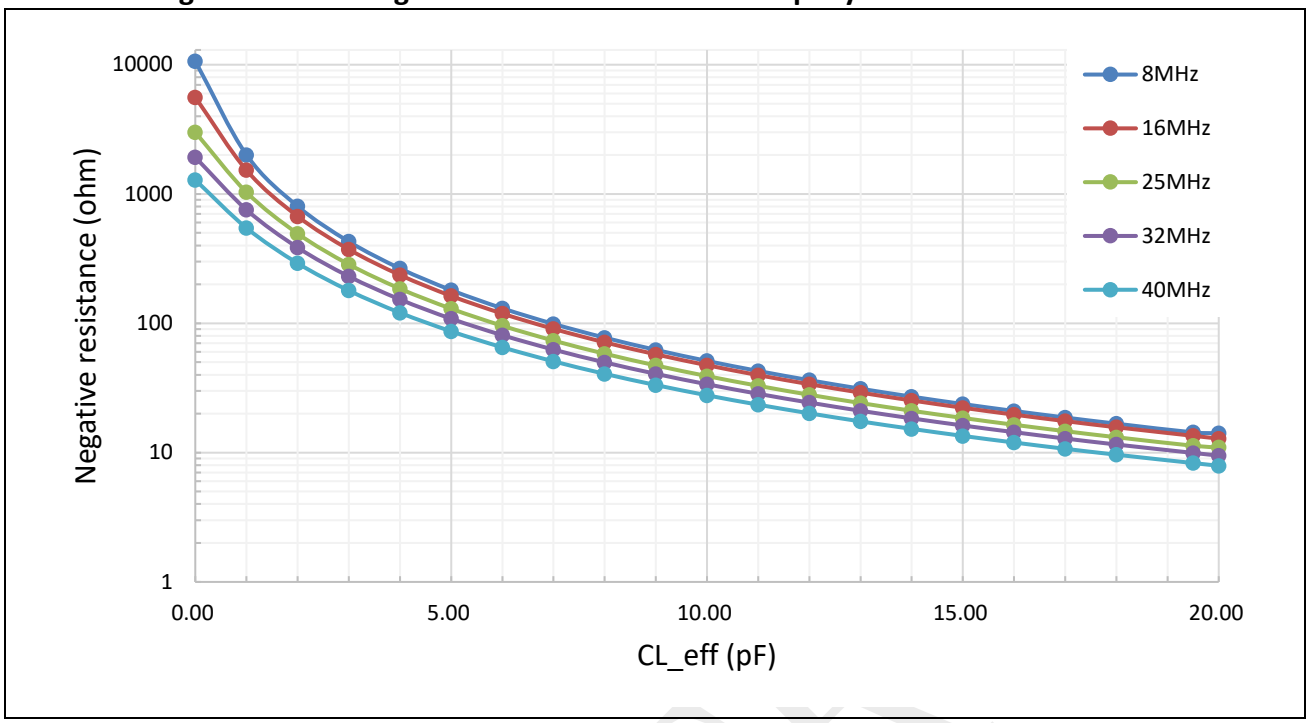
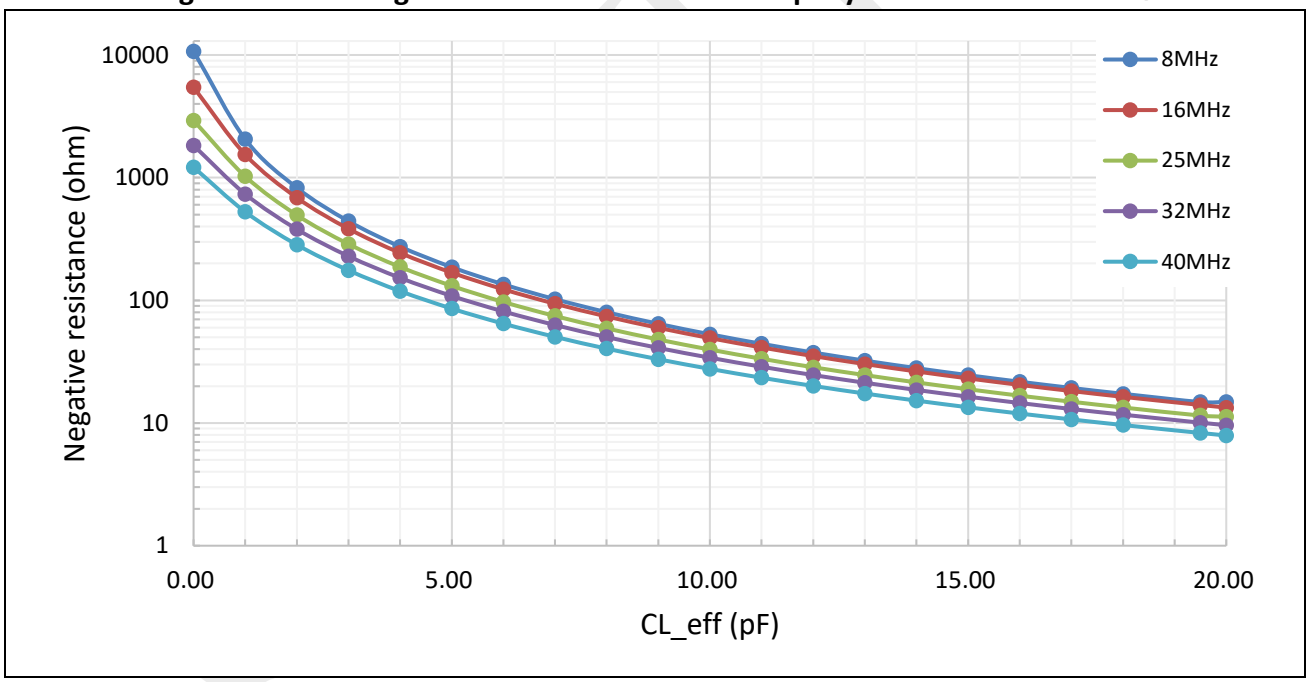


Figure 5-7: The negative resistance of the on-chip crystal oscillator at 125℃



5.10 14-bit ADC characteristics

Table 5-12: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	–	–	bit
F_S	Conversion speed(1)	–	–	–	4	MSPS
V_{AIN}	Input voltage range	–	0	–	V_{VDDA}	V
V_{REF}	Reference voltage	–	1.194	1.2	1.206	V
I_{PAD}	Operational current	V_{VDDA} = 3.3 V	–	17.1	21	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.0	LSB
E_{OFF}	Offset error(2)	With calibration	-2	–	2	LSB
E_{GAIN}	Gain error(2)	With calibration	-4	–	4	LSB
E_{OFF2}	Channel to channel offset	–	-3	–	3	LSB
E_{GAIN2}	Channel to channel gain error	–	-5	–	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	–	–	26	–	ppm/°C
t_{PWRUP}	Power-up time	–	–	–	200	us
$ENOB_{DC}$	DC Noise Floor	–	–	12.0	–	bits
SNR	Signal-to-noise ratio	*f*in = 100kHz Amp = 0.94F_S N = 8192	–	75.5	–	dB
THD	Total harmonic distortion		–	-85.0	–	dB
ENOB	Effective number of bits		–	12.2	–	bits
SFDR	Spurious free dynamic range		–	86.0	–	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	–	–	1.904[3]	–	°C/LSB
T_{OFFSET}	ADC output at 25 °C of the temperature sensor	–	–	162.138	–	LSB

[1] Sampling time = 110ns, conversion time = 140ns

[2] Offset and gain can be calibrated automatically by HW.

[3] Can be reduced to 0.24 °C/LSB by PGA.

5.11 PGA characteristics

Table 5-13: PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	–	0	–	V_{VDDA}	V
V_{OUT}	Output voltage range	–	0.3	–	V_{VDDA} - 0.3	V
R_{IN}	Input impedance	–	–	10	–	MΩ
G	Gain	Single-ended mode	1, 2, 4, 8, 12, 16, 24, 32			–
		Differential mode	2, 4, 8, 16, 24, 32, 48, 64			–
E_{GAIN}	Gain error	Differential Gain = 2	-0.5	–	0.5	%
		Differential Gain = 64	-3	–	3	%
V_{OS}	Offset	–	-5	–	5	mV
T_{OFFSET}	Offset temperature drift	–	–	5	–	uV/ ºC
SR	Slew rate	Single mode and Loading is ADC sampling capacitor	–	20	–	V/us
		Differential mode and Loading is ADC sampling capacitor	–	40	–	V/us
GBW	Gain band width	Single gain = 1	–	40	–	MHz
		Single gain = 8	–	6.8	–	MHz
		Single gain = 32	–	1.7	–	MHz
		Differential gain = 2	–	20	–	MHz
		Differential gain = 16	–	3.4	–	MHz
		Differential gain = 64	–	0.8	–	MHz
t_{SETTLE}	Settle time	Differential gain = 2	–	170[1]	220	ns
		Differential gain = 16	–	400	600	ns
		Differential gain = 64	–	1600	2200	ns
SNR	Signal-to-noise ratio	Differential gain = 2 *f*in = 10kHz Amp = 0.94F_S N = 8192	–	74.0	–	dB
THD	Total harmonic distortion		–	-78.0	–	dB
ENOB	Effective number of bits		–	11.6	–	bit
SFDR	Spurious free dynamic range		–	82.0	–	dB
SNR	Signal-to-noise ratio	Differential gain = 64 *f*in = 10kHz Amp = 0.94F_S N = 8192	–	58.0	–	dB
THD	Total harmonic distortion		–	-80.0	–	dB
ENOB	Effective number of bits		–	9.4	–	bit
SFDR	Spurious free dynamic range		–	63.0	–	dB
I	Current consumption	Only one PGA	–	4.16	5.20	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled with 1LSB (446μV), guarantee by design.

5.12 Analog comparator characteristics

Table 5-14: Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	Common mode input voltage = 1.65V	-10	–	10	mV
V_{HYST}	Hysteresis voltage(12mV)	–	–	13	–	mV
	Hysteresis voltage(24mV)	–	–	26	–	mV
	Hysteresis voltage(36mV)	–	–	42	–	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	–	–	50	–	ns

5.13 Internal 10-bit DAC characteristics

Table 5-15: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
N	resolution	Monotonic	10	–	–	bit
V_{FS}	Full scale value	–	0	–	V_{VDDA}	V
DNL	Differential linearity	–	-0.5	–	0.5	LSB
INL	Integral linearity	–	-1	–	1	LSB
E_{OFF}	Offset error	–	–	5	–	mV
t_{SETTLE}	DAC settling time	Design guarantee	–	–	1	us

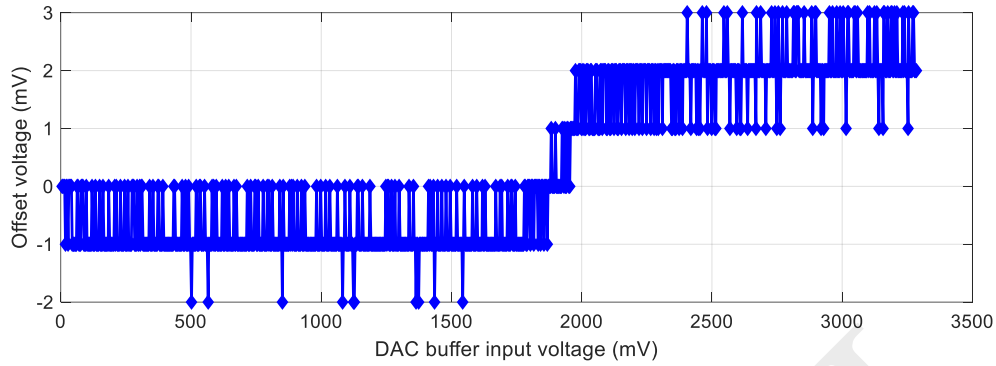
[1] The DAC is used to generate a static voltage as a threshold for the comparator and does not guarantee the performance of the waveform produced by dynamically changing the code value.

5.14 DAC buffer characteristics

Table 5-16: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDA}	Power supply	–	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	–	0.3	–	V_{VDDA} - 0.3	V
t_{SETTLE}	Settling time	Design guarantee	–	1	–	us
E_{OFF}	Offset error	–	–	3	–	mV
C_L	Capacitor load	–	–	–	50	pF
R_L	Resistor load	–	1	–	–	MΩ

Figure 5-8: DAC buffer offset over Input voltage



5.15 Flash memory characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 5-17: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	–	40	–	ns
t_{PROG}	Word (32-bit) program time	–	8	10	us
t_{SE}	Sector erase time	–	0.8	4	ms
t_{CE}	Chip erase time	–	8	10	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100,000	–	cycles
t_{RET}	Data retention duration	T_J = 85 °C	10	–	years

5.16 Electrical sensitivity characteristics

Table 5-18: ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	–	500	V
			Corner Pin	750	V

Table 5-19: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{VDD} = 3.63V, V_{VCAP12} = 1.32V	100	mA

5.17 Moisture sensitivity characteristics

Table 5-20: Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	–	Level 3	–

5.18 Thermal resistance characteristics

Table 5-21: Thermal resistance characteristics (LQFP80 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	9.82	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	57.58	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	41.84	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-22: Thermal resistance characteristics (LQFP64 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	19.03	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	76.52	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	58.81	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-23: Thermal resistance characteristics (LQFP52 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	18.69	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	68.42	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	54.61	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-24: Thermal resistance characteristics (LQFP48 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	16.84	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	72.15	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	52.37	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-25: Thermal resistance characteristics (QFN52 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	10.03	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	57.93	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	34.49	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.19 SPI characteristics

Table 5-26: SPI characteristics

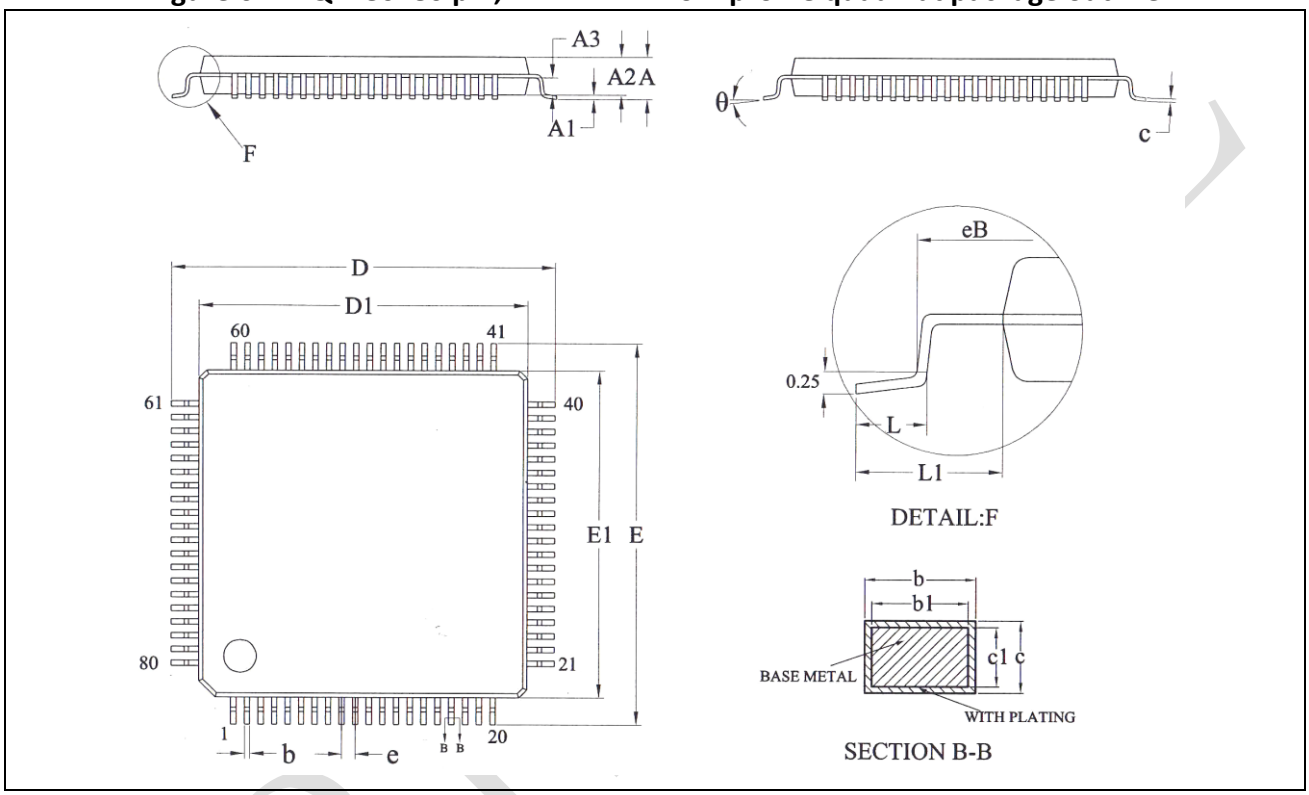
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	–	–	–	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	–	10	–	–	ns
$t_{SCLK(L)}$	SCLK clock low time	–	10	–	–	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	–	–	–	9.5	ns
$t_{H(MO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(MI)}$	Data input setup time	–	6	–	–	ns
$t_{H(MI)}$	Data input hold time	–	2	–	–	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	–	5.6	–	–	ns
$t_{H(SFRM)}$	SFRM enable hold time	–	1.5	–	–	ns
$t_{A(SO)}$	Data output access time	–	4	–	10	ns
$t_{DIS(SO)}$	Data output disable time	–	4	–	10	ns
$t_{V(SO)}$	Data output valid time	–	–	–	9.5	ns
$t_{H(SO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(SI)}$	Data input setup time	–	6	–	–	ns
$t_{H(SI)}$	Data input hold time	–	2	–	–	ns

6 Package information

The package type of SPC2168 can be 80-pin LQFP, 64-pin LQFP, 52-pin LQFP, 48-pin LQFP or 52-pin QFN. The detail information is as below.

6.1 LQFP80

Figure 6-1: LQFP80–80 pin, 12 x 12 mm low-profile quad flat package outline

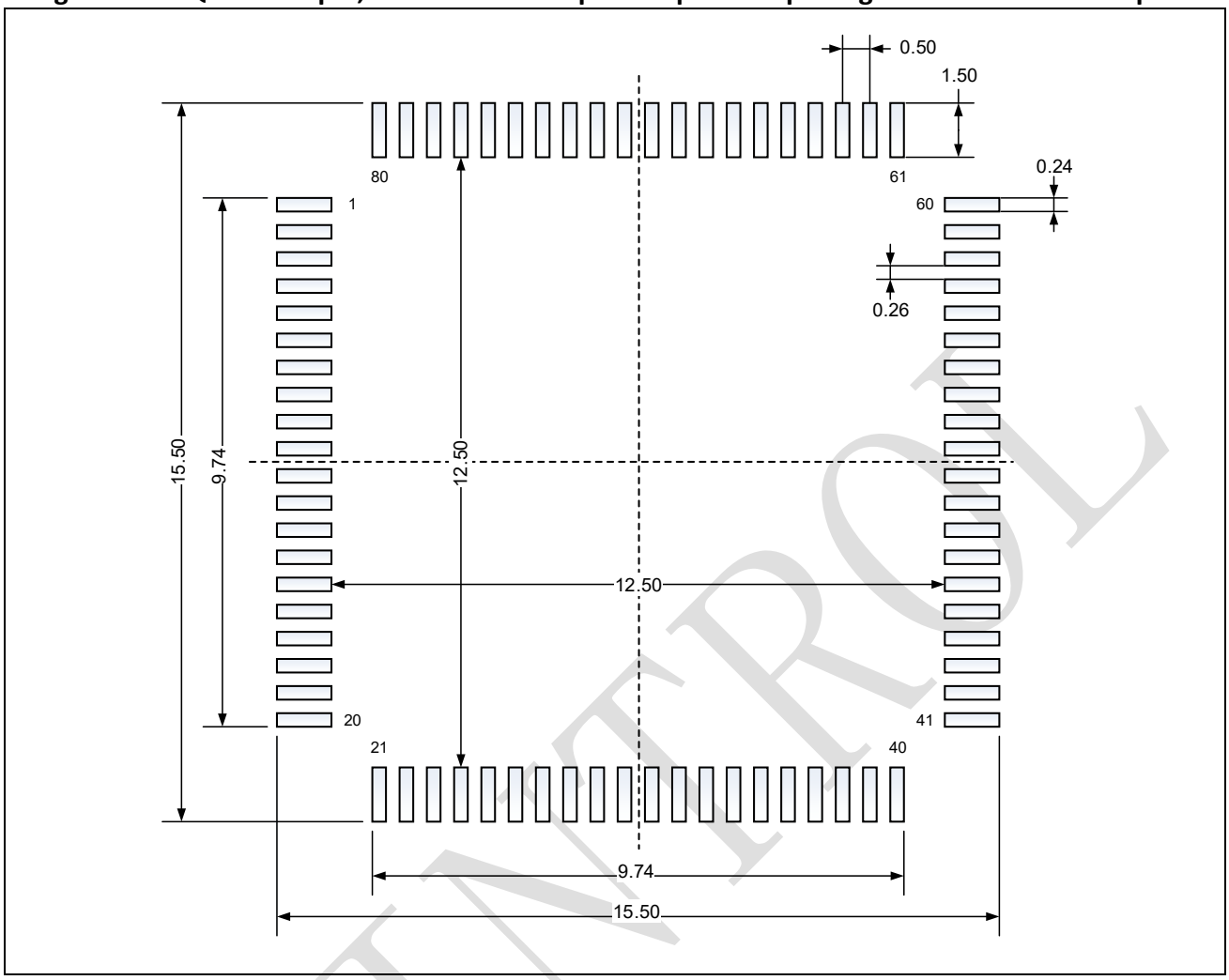


[1] Drawing is not to scale.

Table 6-1: LQFP80–80 pin, 12 x 12 mm low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.26
b1	0.17	0.20	0.23
c	0.13	–	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	–	13.25
e	–	0.50	–
L	0.45	0.60	0.75
L1	–	1.00REF	–
θ	0	–	7°

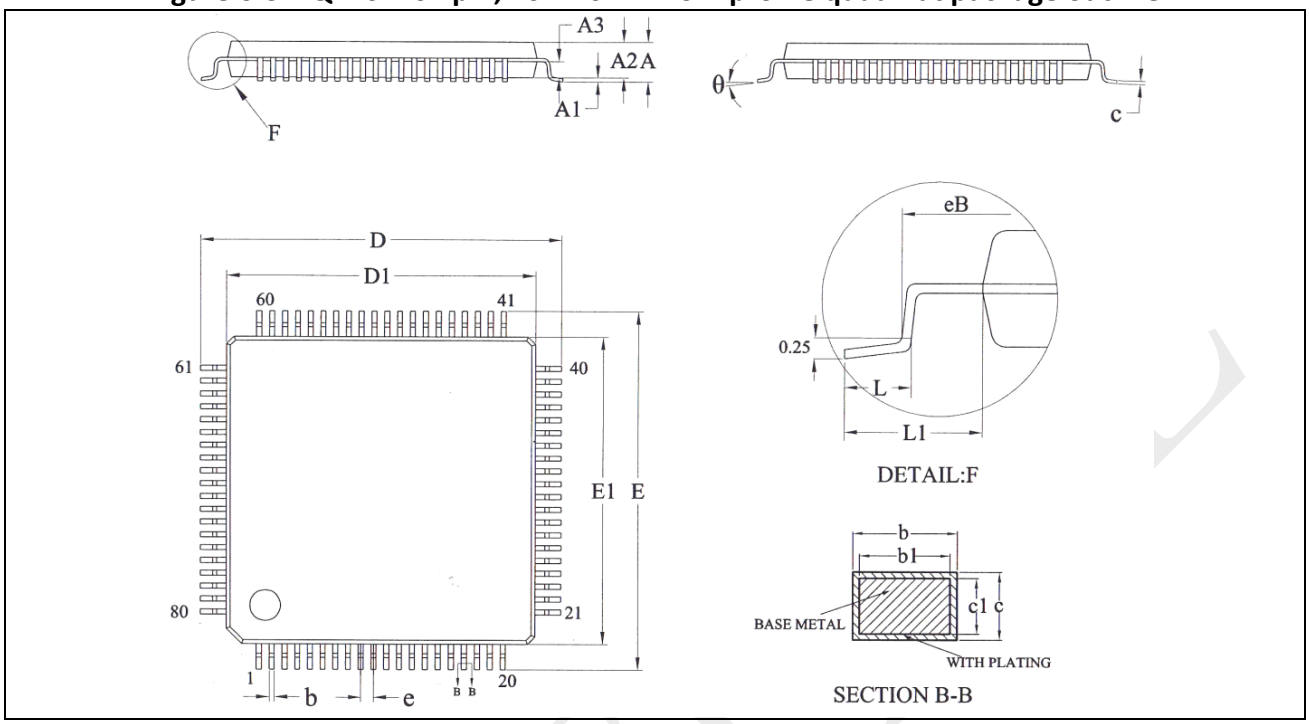
Figure 6-2: LQFP80–80 pin, 12 x 12 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

6.2 LQFP64

Figure 6-3: LQFP64–64 pin, 10 x 10 mm low-profile quad flat package outline

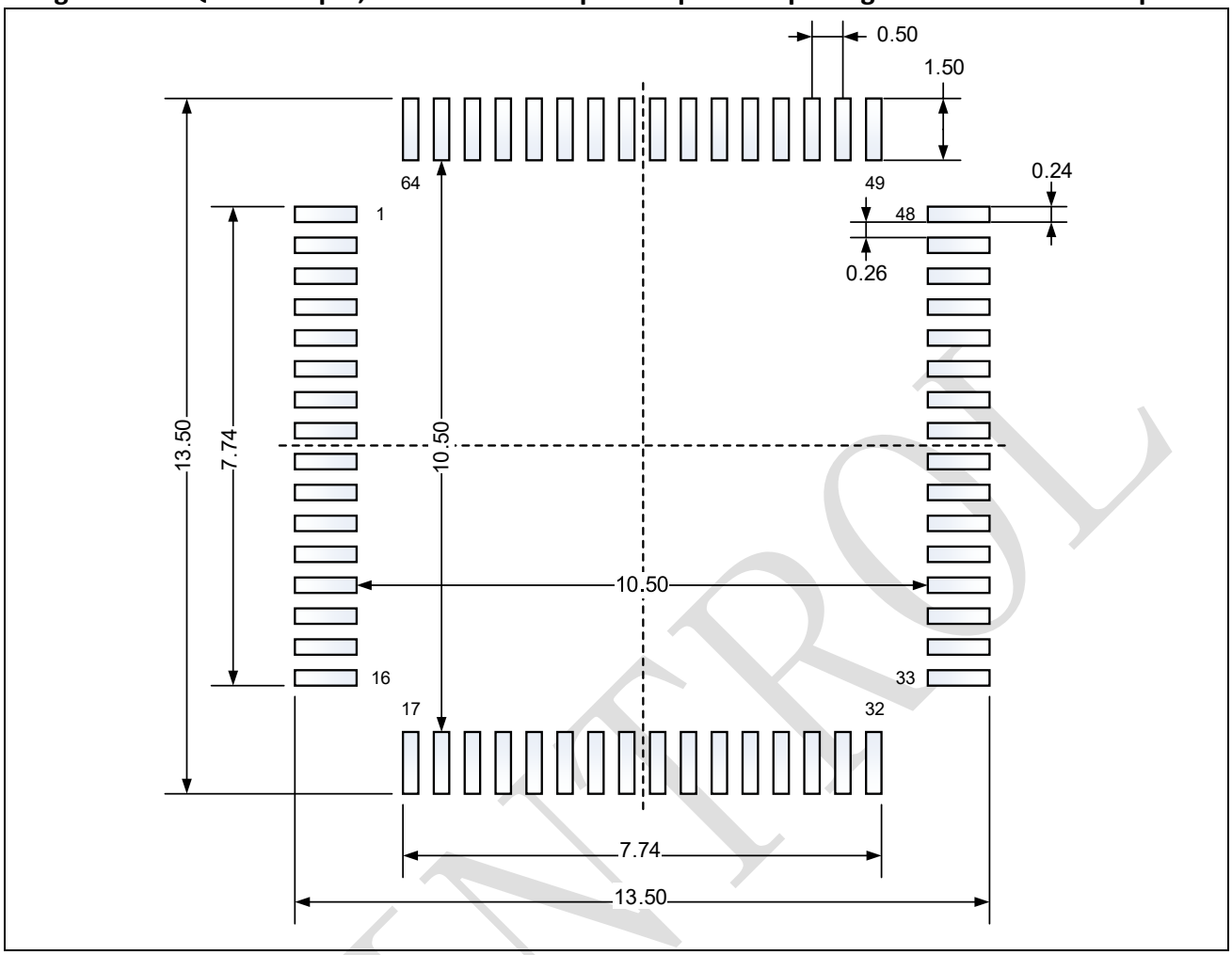


[1] Drawing is not to scale.

Table 6-2: LQFP64–64 pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.26
b1	0.17	0.20	0.23
c	0.13	–	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	–	11.25
e	–	0.50	–
L	0.45	0.60	0.75
L1	–	1.00REF	–
θ	0	–	7°

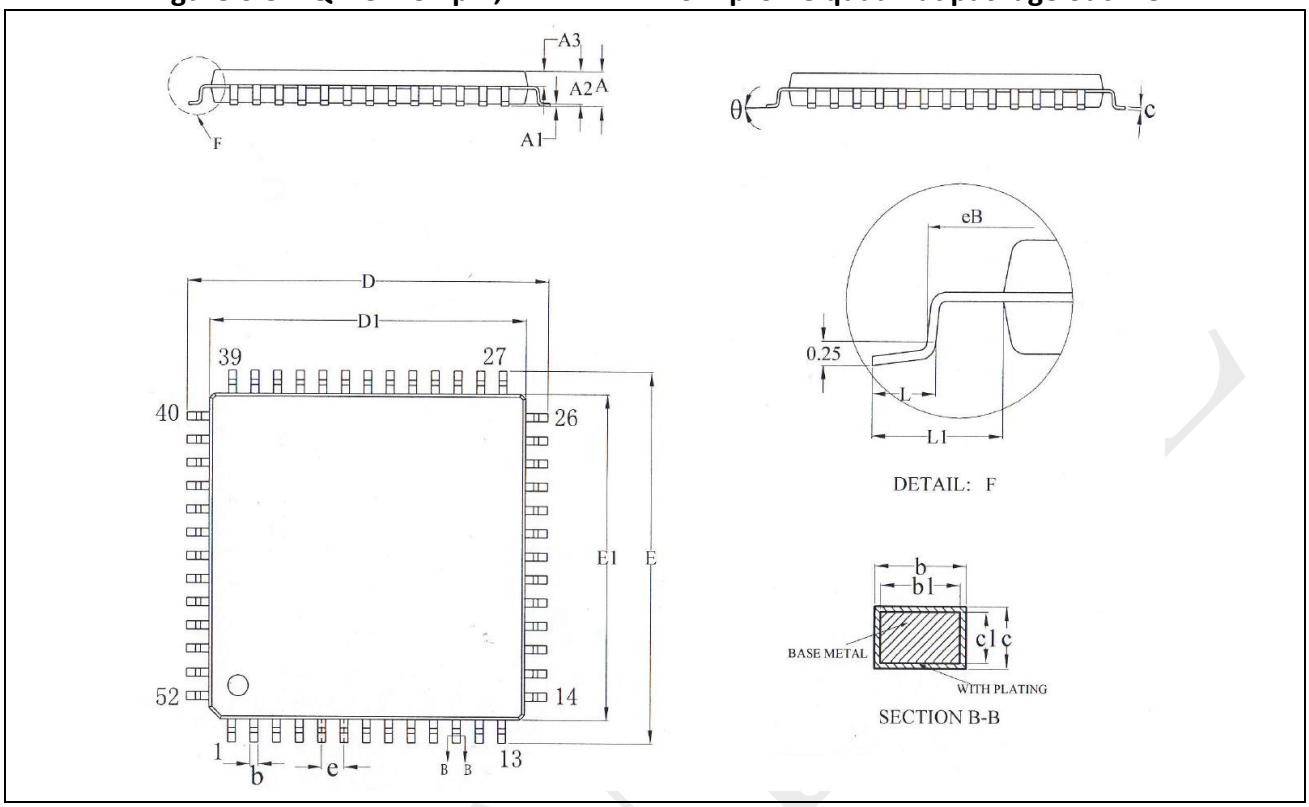
Figure 6-4: LQFP64–64 pin, 10 x 10 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

6.3 LQFP52

Figure 6-5: LQFP52–52 pin, 14 x 14 mm low-profile quad flat package outline

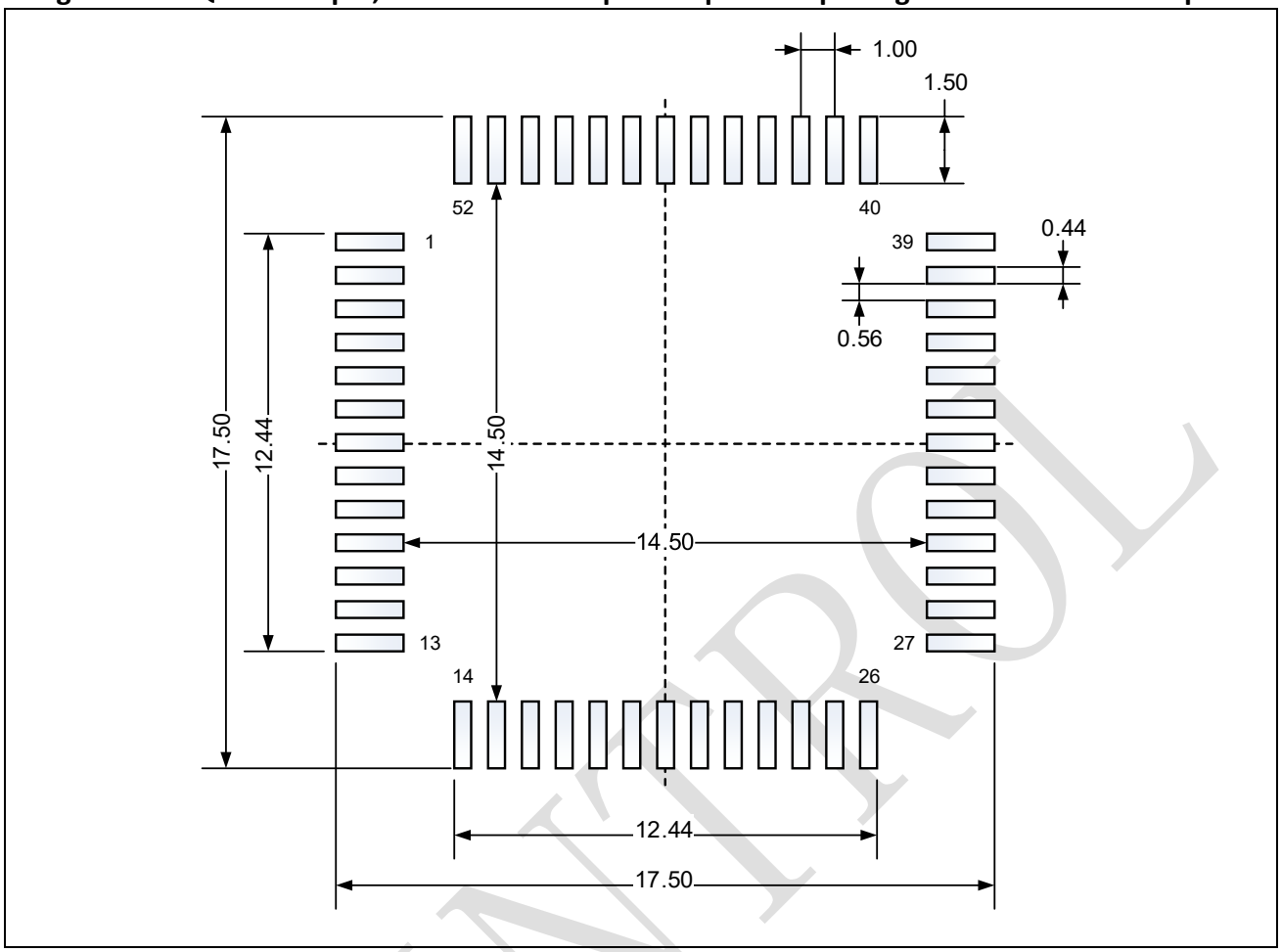


[1] Drawing is not to scale.

Table 6-3: LQFP52–52 pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.38	–	0.46
b1	0.37	0.40	0.43
c	0.13	–	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	–	15.35
e	–	1.00	–
L	0.45	–	0.75
L1	–	1.00REF	–
θ	0	–	7°

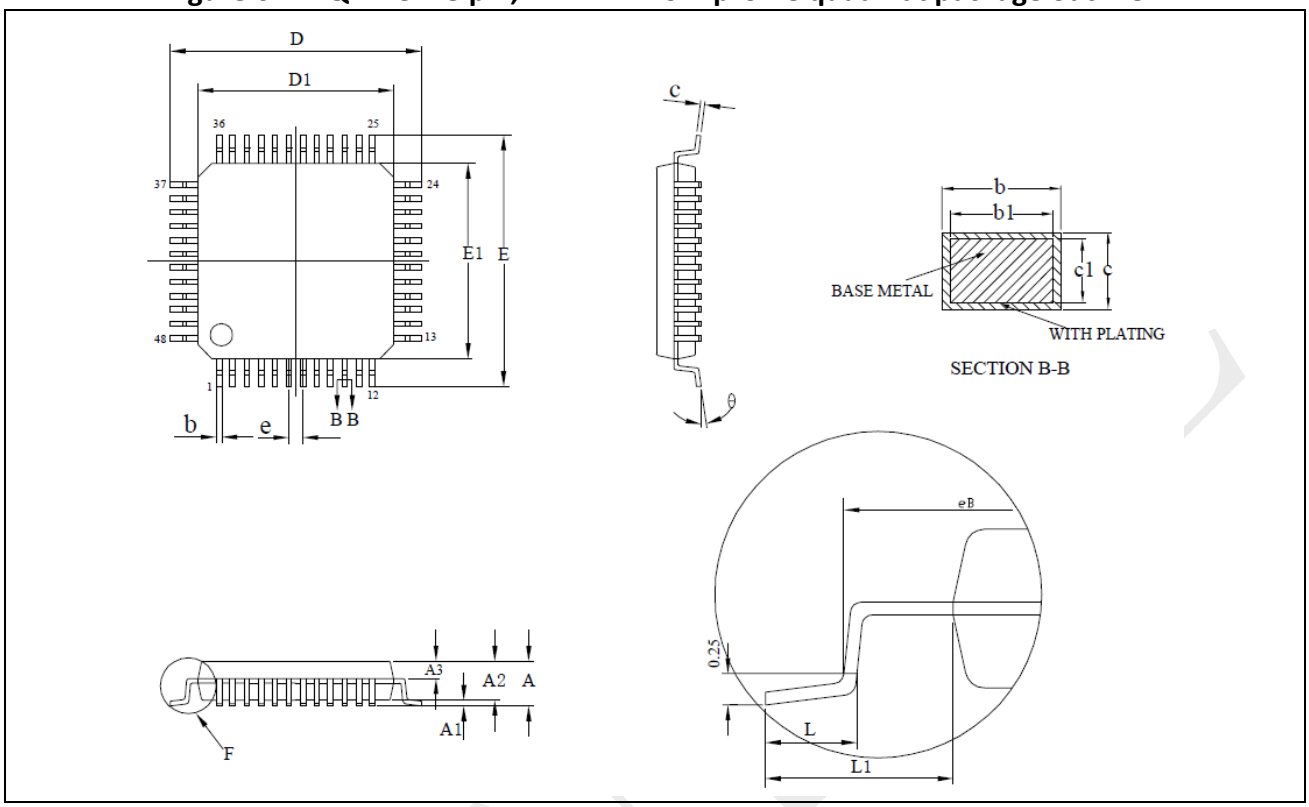
Figure 6-6: LQFP52–52 pin, 14 x 14 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

6.4 LQFP48

Figure 6-7: LQFP48–48 pin, 7 x 7 mm low-profile quad flat package outline

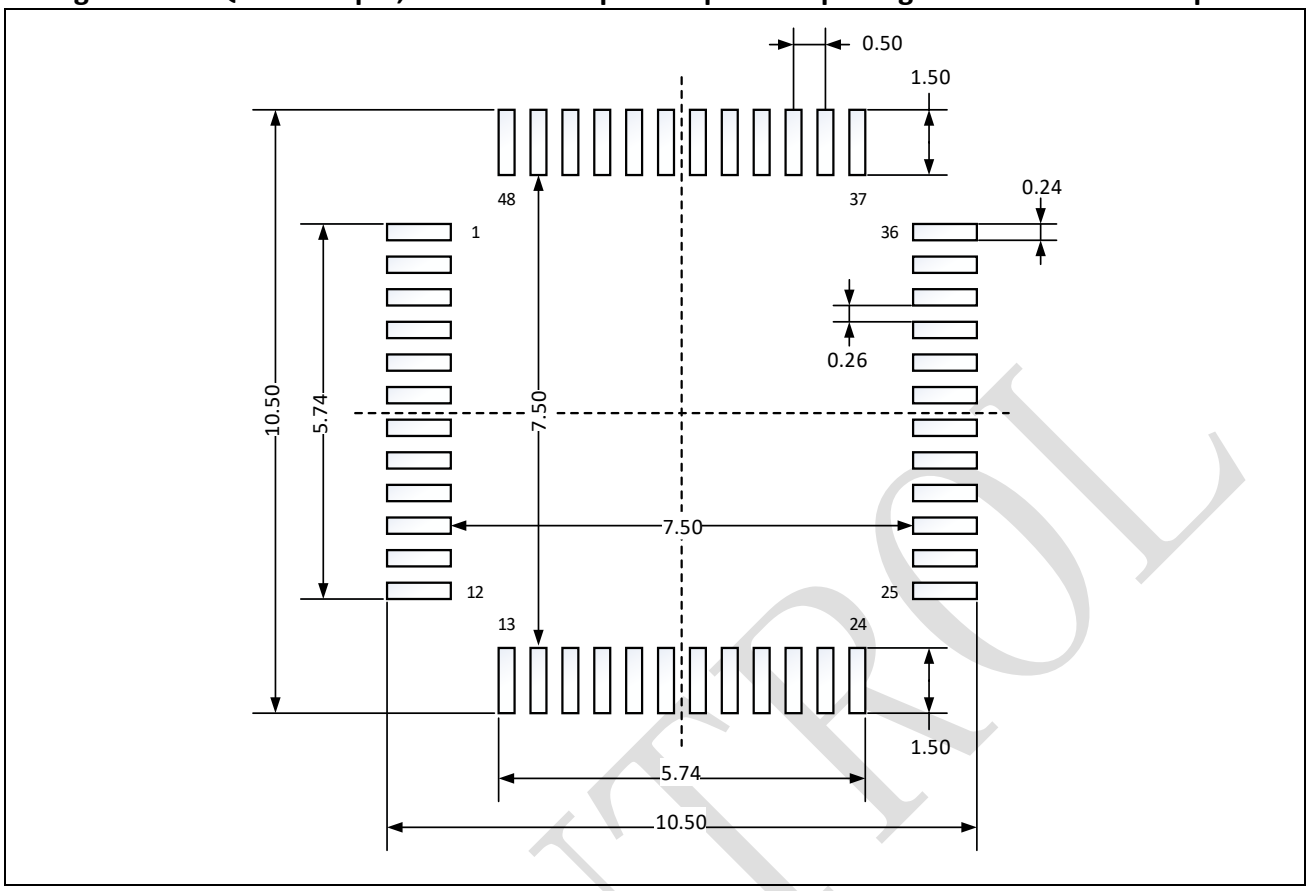


[1] Drawing is not to scale.

Table 6-4: LQFP48–48 pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	–	0.27
b1	0.18	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	–	8.25
e	–	0.5	–
L	0.4	–	0.75
L1	–	1.00	–
θ	0	–	7°

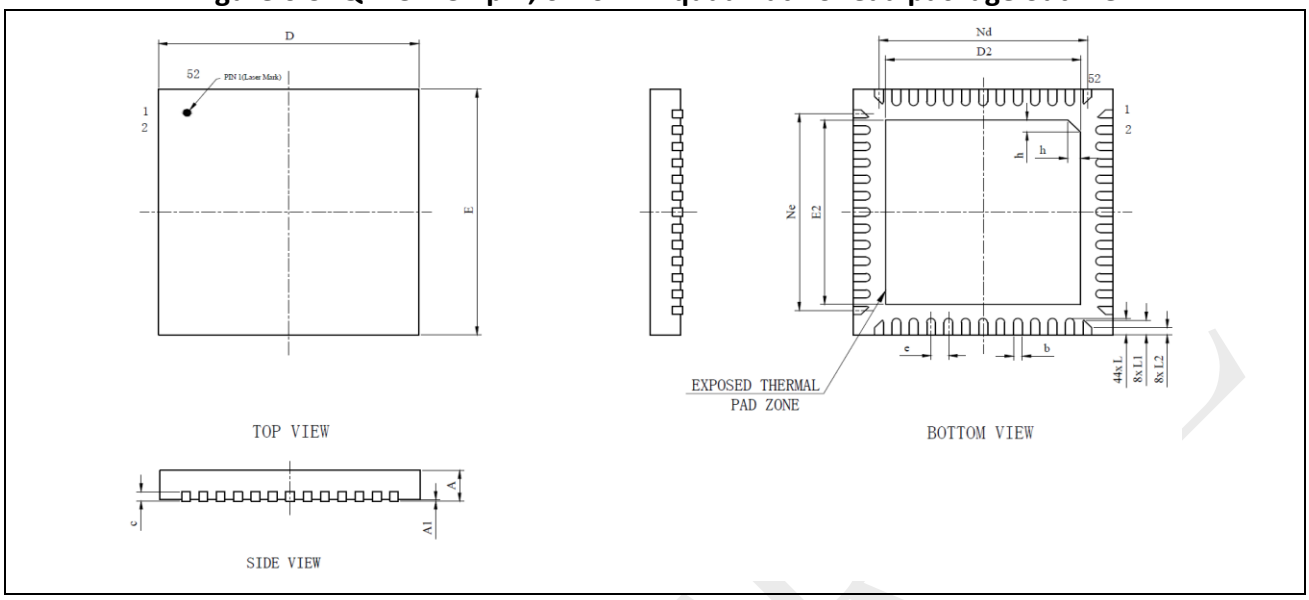
Figure 6-8: LQFP48–48 pin, 7 x 7 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

6.5 QFN52

Figure 6-9: QFN52–52 pin, 6 x 6 mm quad flat no-lead package outline

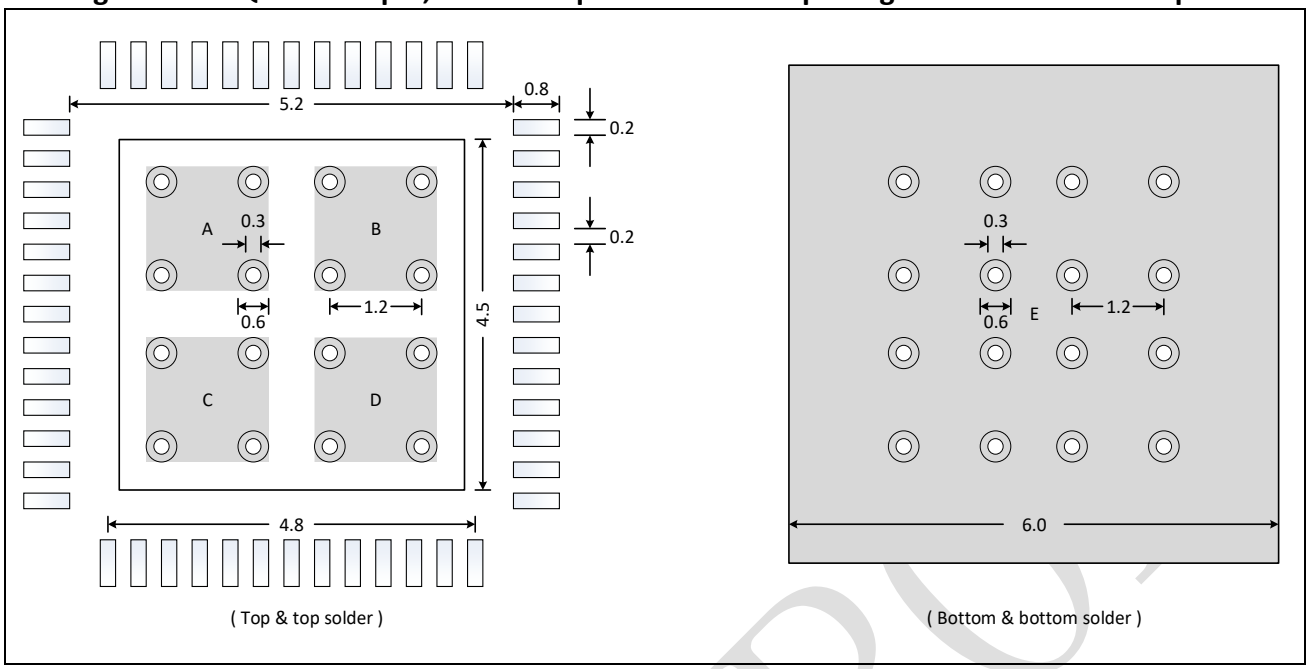


[1] Drawing is not to scale.

Table 6-5: QFN52–52 pin, 6 x 6 mm quad flat no-lead package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	–	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40		
Nd	4.80		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35

Figure 6-10: QFN52–52 pin, 6 x 6 mm quad flat no-lead package recommended footprint



[1] Dimensions are expressed in millimeters.

[2] The A, B, C, D areas on the top layer should brush solder paste, and E area on bottom layer can either brush solder paste or not.

7 Ordering information

Table 7-1: Ordering information

Ordering Number	Flash	SRAM	Max f_{CPU}	Package	Temperature Range	SPQ[1]	Packing
SPC2168APE80	512KB	80KB	200 MHz	LQFP80	Industrial -40 °C to +125 °C	1190	Tray
SPC2168LAPE80	256KB	80KB	200 MHz	LQFP80	Industrial -40 °C to +125 °C	1190	Tray
SPC2168ZAPE80	128KB	80KB	200 MHz	LQFP80	Industrial -40 °C to +125 °C	1190	Tray
SPC2168APE64	512KB	80KB	200 MHz	LQFP64	Industrial -40 °C to +125 °C	1600	Tray
SPC2168LAPE64	256KB	80KB	200 MHz	LQFP64	Industrial -40 °C to +125 °C	1600	Tray
SPC2168APE52[2]	512KB	80KB	200 MHz	LQFP52	Industrial -40 °C to +125 °C	900	Tray
SPC2168APE48[3]	512KB	80KB	200 MHz	LQFP48	Industrial -40 °C to +125 °C	2500	Tray
SPC2168API52	512KB	80KB	200 MHz	QFN52	Industrial -40 °C to +125 °C	4900	Tray

[1] SPQ = Standard Pack Quantity.

[2] SPC2168APE52 is not officially on product line now and is subject to change.

[3] SPC2168APE48 is not officially on product line now and is subject to change.

7.1 Rule of ordering number

Figure 7-1: Rule of ordering number